

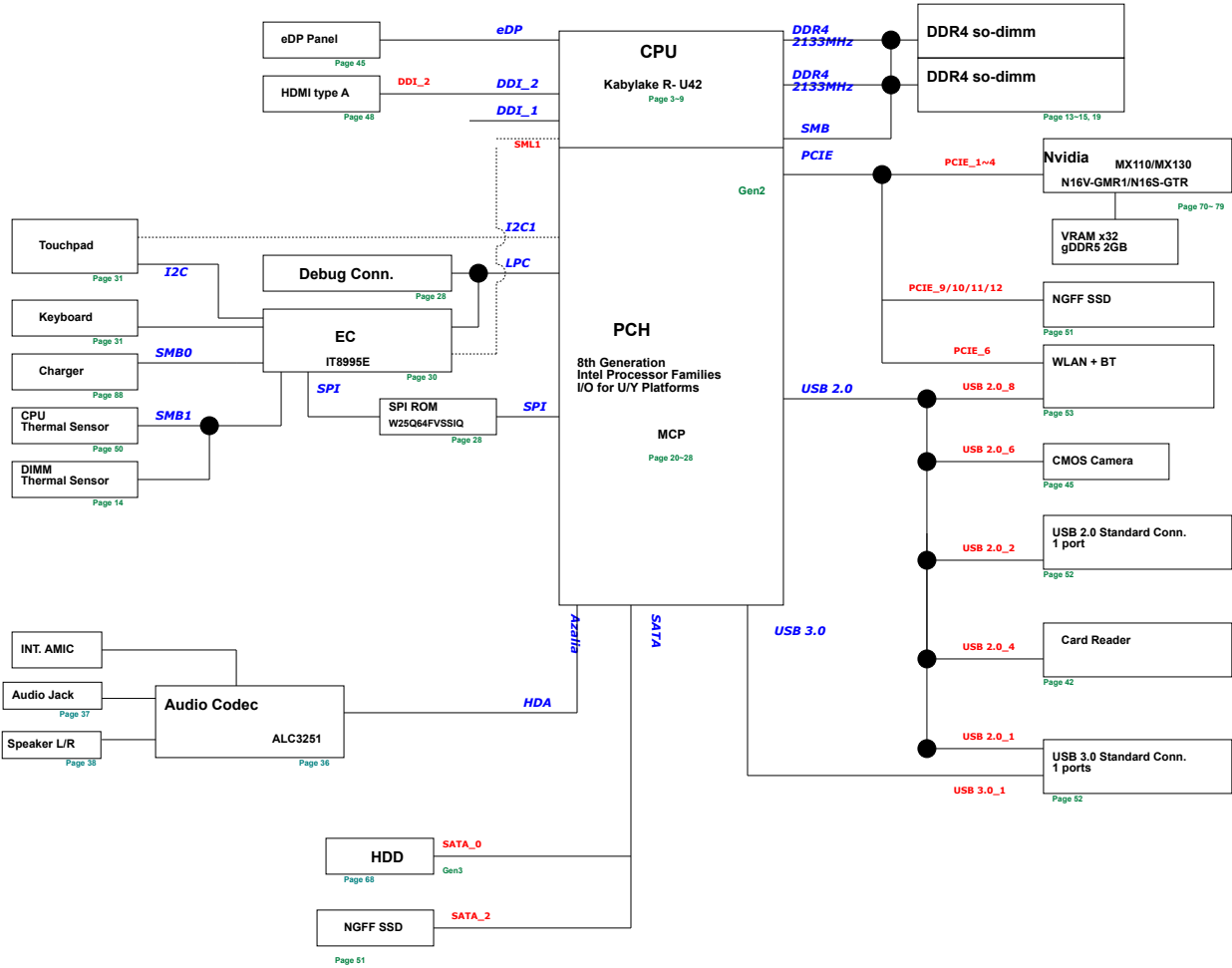
X407UAR/UBR/UFR SCHEMATIC Revision 1.0

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071	VGA_nVIDIA_N16V/S_FB-IF
072	VGA_nVIDIA_N16V/S_FB-DDR3
073	VGA_nVIDIA_N16V/S_VDD
074	VGA_nVIDIA_N16V/S_DISPLAY
075	VGA_nVIDIA_N16V/S_ROM,XTAL
076	VGA_nVIDIA_N16V/S_GPIO
077	VGA_nVIDIA_N16V/S_POWER
080	PW_IMVP8 (1) (RT3601BCGQW)
081	PW_IMVP8 (2) (RT3601BCGQW)
083	PW_+1.0VSUS / +1.8VSUS
084	PW_+1.2VS
086	PW_1.35V/+0.675VS (UP9011Q)
087	PW_+3VADSW/+5VSUS (RT8249C)
088	PW_LOAD SWITCH
089	PW_CHARGER(BQ24780)
090	PW_PROTECTION
091	PW_DGPU_2PHASE(RT8815A)

BLOCK DIAGRAM

Non Connected Standby

(UAR : UMA) (45W) (Power BOM)
(UBR : DGPU = Nvidia N16V-GMR1, MX110) (65W) (Power BOM)
(UFR : DGPU = Nvidia N16S-GTR, MX130) (65W) (Power BOM)





Power
+VCCGT +VCCCORE +VCCST
+1.0VSUS / +1.8VSUS
+0.95VSG +VCCPRIM_CORE
+1.2V / +VTT / +2.5V
+3VADSW/+5VSUS
Load Switch
Charger
+VDDC

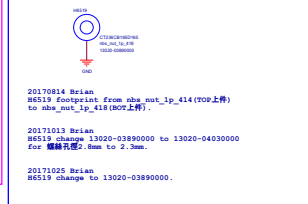
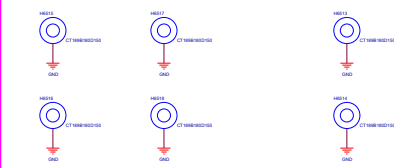
CPU XDP	Discharge Circuit	DC & BATT. Conn.	PWM Fan
Reset Circuit	Skew Holes		

+1.8VSUS [For PCH]

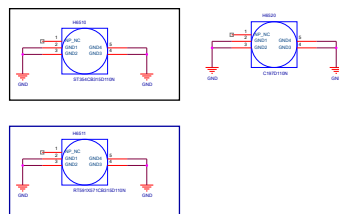
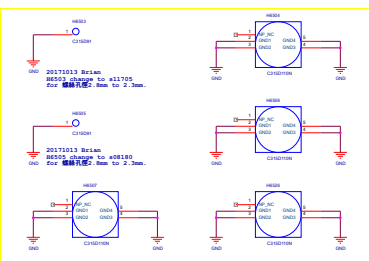
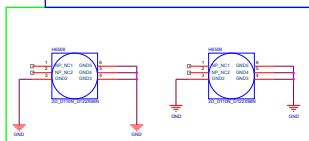
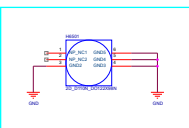


		Project Name		Rev
		X540UVK		R1.0
Title : PW_+1.2VS				
Size	Dept.:		Engineer:	
A3	NB Power Team		Andy	
Date: Wednesday, March 07, 2018			Sheet	85 of 102

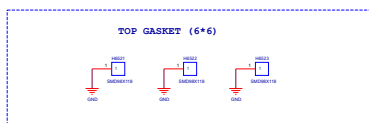
		Project Name		Rev
		X540UVK		R1.0
Title : POWER_+VGFX_CORE				
Size Custom	Dept.: NB Power Team		Engineer:	Andy
Date: Wednesday, March 07, 2018			Sheet	86 of 102



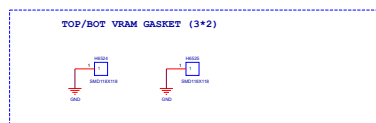
20170814 Brian
H6519 footprint from abn_nut_1p_414 (TOP 上料)
to abn_nut_1p_418 (TOP 上料)
20171013 Brian
H6519 change 13020-03890000 to 13020-04030000
For 螺丝孔距 2.5mm to 2.3mm.
20171025 Brian
H6519 change to 13020-03890000.



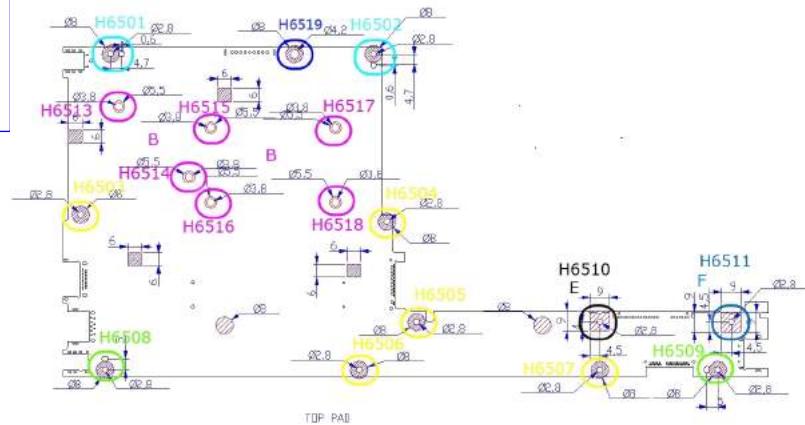
20180117 Brian
Add H6526 for RM DIMM-door.



TOP GASKET (6*6)

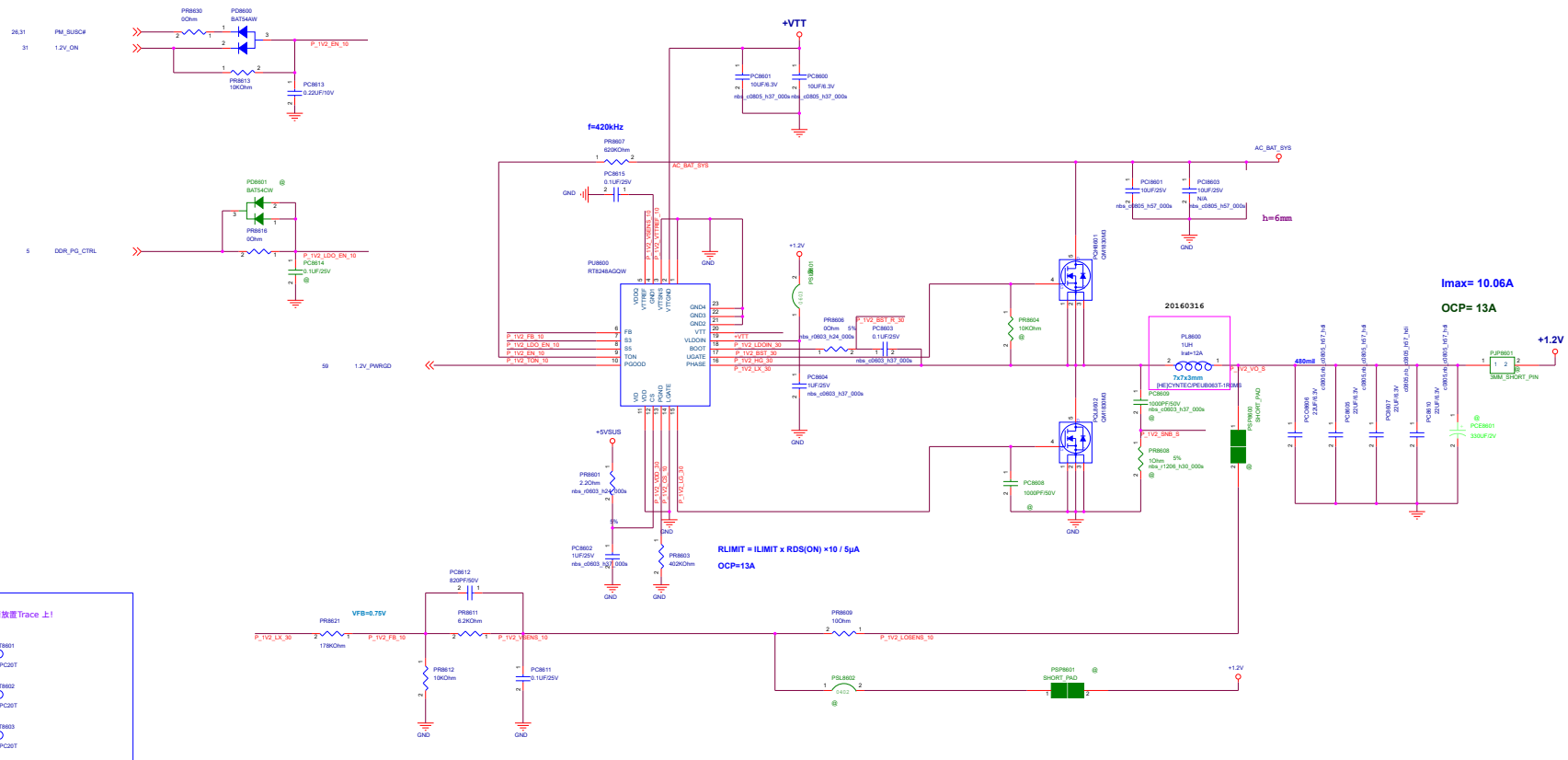


TOP/BOT VRAM GASKET (3*2)

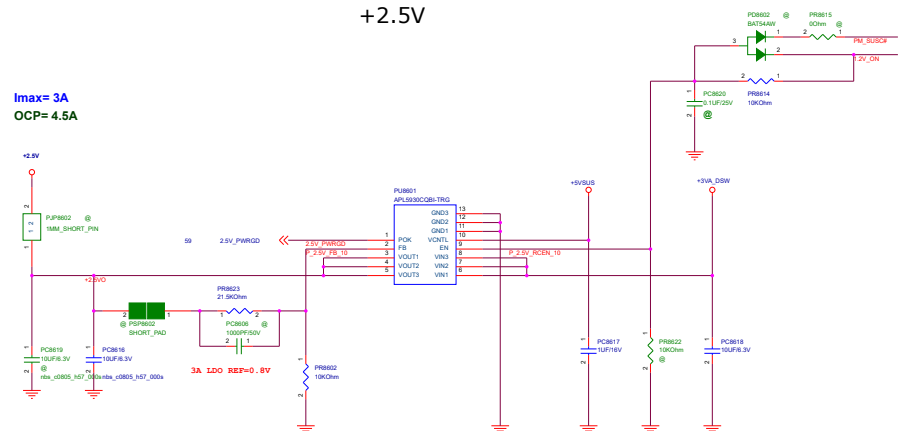


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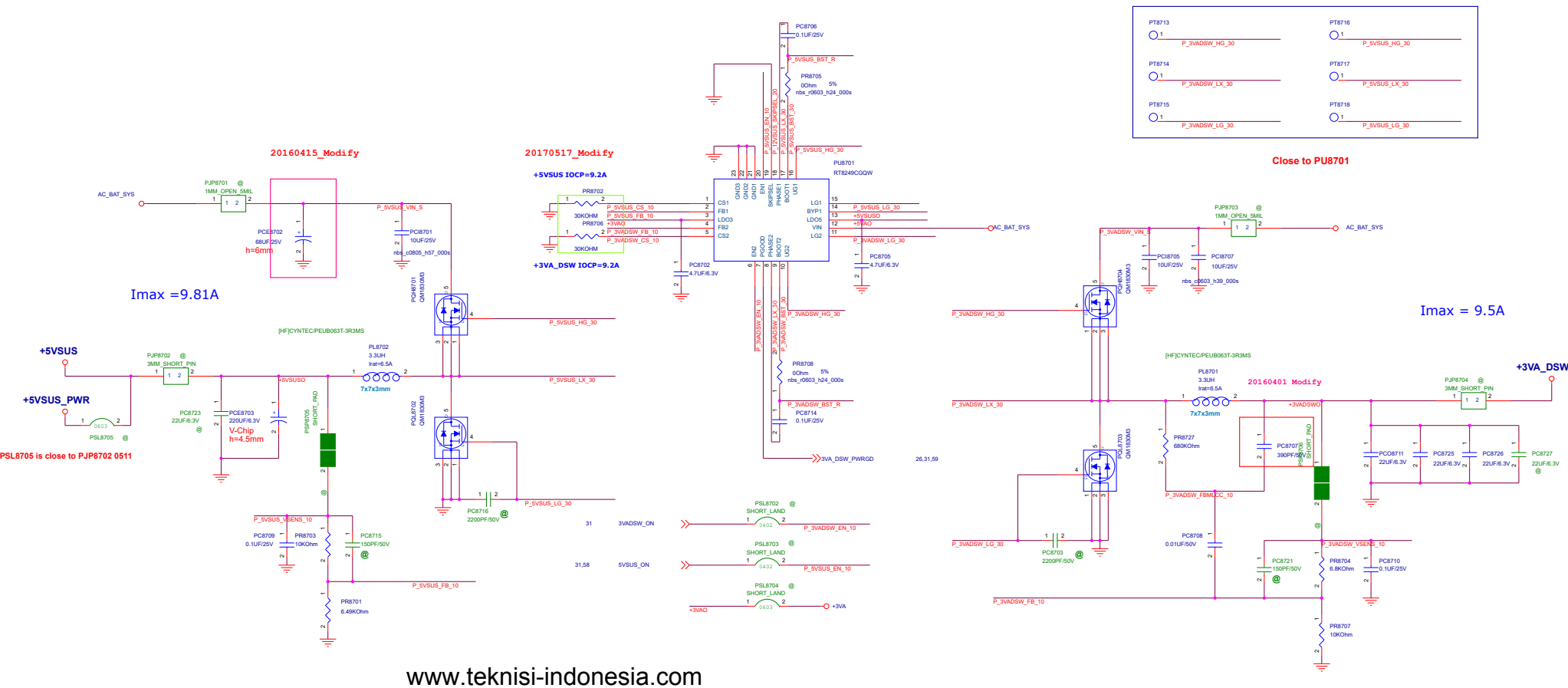
+1.2V / +VTT / +2.5V[For Memory]



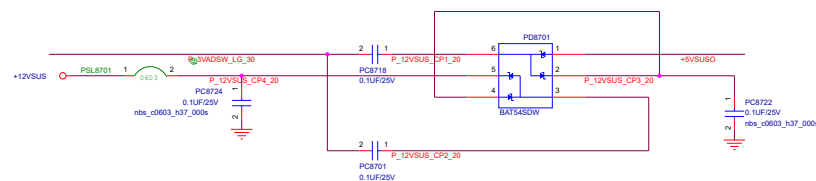
+2.5V



+3VA_DSW / +5VSUS [System Power]

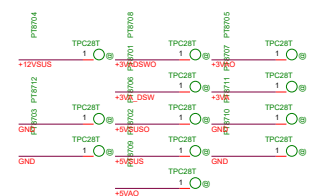


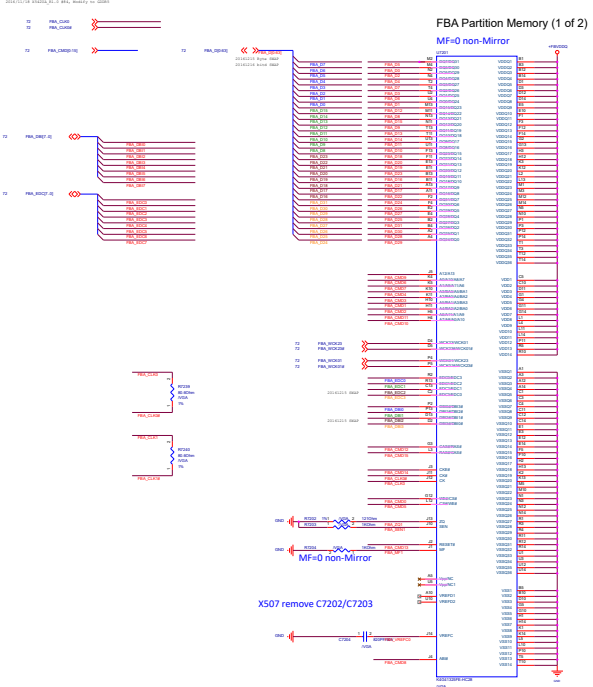
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Adaptor Mode (MVP8)								Battery Mode (MVP8)							
	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+		S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	1	-	1	-	1	PS_ON	1	-	-	1	-	1	1
3VADSW_ON	1	-	1	-	1	-	1	3VADSW_ON	1	-	-	1	0	0	0
3VSUS_ON	1	-	1	-	0	-	0	3VSUS_ON	1	-	-	0	0	0	0
5VSUS_ON	1	-	1	-	1	-	1	5VSUS_ON	1	-	-	1	0	0	1
1.35V_ON	1	-	1	-	0	-	0	1.35V_ON	1	-	-	1	0	0	0
SUSC_EC#	1	-	1	-	0	-	0	SUSC_EC#	1	-	-	0	0	0	0
SUSC_EC#	1	-	0	-	0	-	0	SUSC_EC#	1	-	-	0	0	0	0





GDDR5 X32

Table 7-4. GDDR5 Mode H Mapping

GB2-64, GB28-64, GB48-128	Channel 0 0..31	GB2-64, GB28-64, GB48-128	Channel 1 32..63
CMD0	CS*	CMD16	CS*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	AB*	CMD24	AB*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RA*	CMD28	RA*
CMD13	RS*	CMD29	RS*
CMD14	CKE*	CMD30	CKE*
CMD15	CAS*	CMD31	CAS*

GB2-64, GB28-64, GB48-128	Channel 0 64..127
CMD32	Hot-Reset
CMD33	Hot-Reset
CMD34	DEBUG0
CMD35	DEBUG1

Notes:
1. Not available in GB2-64 and GB28-64 packages.
2. GPU debug pins, not connected to DRAM. See section 7.1.13.



7.1.12.1 YREF-D

YREF-D pins can be left floating.

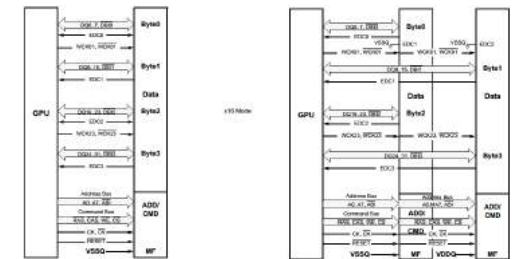
7.1.12.2 YREF-C

YREF-C connections for the x16 mode are shown in Figure 7-8.

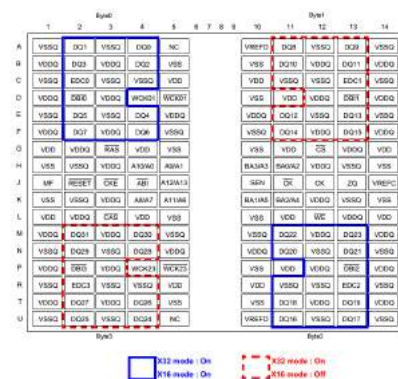
Table 7-14. YREF Configuration

Configuration	Requirement	Note:
x32	Share one Yref-C circuit for two memory parts.	GDDR5 DRAMs have internal YREFs for DQ, A0, B0, C0, D0, E0, F0, G0, H0, I0, J0, K0, L0, M0, N0, O0, P0, Q0, R0, S0, T0, U0, V0, W0, X0, Y0, Z0, AA0, AB0, AC0, AD0, AE0, AF0, AG0, AH0, AI0, AJ0, AK0, AL0, AM0, AN0, AO0, AP0, AQ0, AR0, AS0, AT0, AU0, AV0, AW0, AX0, AY0, AZ0, BA0, BB0, BC0, BD0, BE0, BF0, BG0, BH0, BI0, BJ0, BK0, BL0, BM0, BN0, BO0, BP0, BQ0, BR0, BS0, BT0, BU0, BV0, BW0, BX0, BY0, BZ0, CA0, CB0, CC0, CD0, CE0, CF0, CG0, CH0, CI0, CJ0, CK0, CL0, CM0, CN0, CO0, CP0, CQ0, CR0, CS0, CT0, CU0, CV0, CW0, CX0, CY0, CZ0, DA0, DB0, DC0, DD0, DE0, DF0, DG0, DH0, DI0, DJ0, DK0, DL0, DM0, DN0, DO0, DP0, DQ0, DR0, DS0, DT0, DU0, DV0, DW0, DX0, DY0, DZ0, EA0, EB0, EC0, ED0, EE0, EF0, EG0, EH0, EI0, EJ0, EK0, EL0, EM0, EN0, EO0, EP0, EQ0, ER0, ES0, ET0, EU0, EV0, EW0, EX0, EY0, EZ0, FA0, FB0, FC0, FD0, FE0, FF0, FG0, FH0, FI0, FJ0, FK0, FL0, FM0, FN0, FO0, FP0, FQ0, FR0, FS0, FT0, FU0, FV0, FW0, FX0, FY0, FZ0, GA0, GB0, GC0, GD0, GE0, GF0, GG0, GH0, GI0, GJ0, GK0, GL0, GM0, GN0, GO0, GP0, GQ0, GR0, GS0, GT0, GU0, GV0, GW0, GX0, GY0, GZ0, HA0, HB0, HC0, HD0, HE0, HF0, HG0, HH0, HI0, HJ0, HK0, HL0, HM0, HN0, HO0, HP0, HQ0, HR0, HS0, HT0, HU0, HV0, HW0, HX0, HY0, HZ0, IA0, IB0, IC0, ID0, IE0, IF0, IG0, IH0, II0, IJ0, IK0, IL0, IM0, IN0, IO0, IP0, IQ0, IR0, IS0, IT0, IU0, IV0, IW0, IX0, IY0, IZ0, JA0, JB0, JC0, JD0, JE0, JF0, JG0, JH0, JI0, JJ0, JK0, JL0, JM0, JN0, JO0, JP0, JQ0, JR0, JS0, JT0, JU0, JV0, JW0, JX0, JY0, JZ0, KA0, KB0, KC0, KD0, KE0, KF0, KG0, KH0, KI0, KJ0, KK0, KL0, KM0, KN0, KO0, KP0, KQ0, KR0, KS0, KT0, KU0, KV0, KW0, KX0, KY0, KZ0, LA0, LB0, LC0, LD0, LE0, LF0, LG0, LH0, LI0, LJ0, LK0, LL0, LM0, LN0, LO0, LP0, LQ0, LR0, LS0, LT0, LU0, LV0, LW0, LX0, LY0, LZ0, MA0, MB0, MC0, MD0, ME0, MF0, MG0, MH0, MI0, MJ0, MK0, ML0, MM0, MN0, MO0, MP0, MQ0, MR0, MS0, MT0, MU0, MV0, MW0, MX0, MY0, MZ0, NA0, NB0, NC0, ND0, NE0, NF0, NG0, NH0, NI0, NJ0, NK0, NL0, NM0, NO0, NP0, NQ0, NR0, NS0, NT0, NU0, NV0, NW0, NX0, NY0, NZ0, OA0, OB0, OC0, OD0, OE0, OF0, OG0, OH0, OI0, OJ0, OK0, OL0, OM0, ON0, OO0, OP0, OQ0, OR0, OS0, OT0, OU0, OV0, OW0, OX0, OY0, OZ0, PA0, PB0, PC0, PD0, PE0, PF0, PG0, PH0, PI0, PJ0, PK0, PL0, PM0, PN0, PO0, PP0, PQ0, PR0, PS0, PT0, PU0, PV0, PW0, PX0, PY0, PZ0, QA0, QB0, QC0, QD0, QE0, QF0, QG0, QH0, QI0, QJ0, QK0, QL0, QM0, QN0, QO0, QP0, QQ0, QR0, QS0, QT0, QU0, QV0, QW0, QX0, QY0, QZ0, RA0, RB0, RC0, RD0, RE0, RF0, RG0, RH0, RI0, RJ0, RK0, RL0, RM0, RN0, RO0, RP0, RQ0, RR0, RS0, RT0, RU0, RV0, RW0, RX0, RY0, RZ0, SA0, SB0, SC0, SD0, SE0, SF0, SG0, SH0, SI0, SJ0, SK0, SL0, SM0, SN0, SO0, SP0, SQ0, SR0, SS0, ST0, SU0, SV0, SW0, SX0, SY0, SZ0, TA0, TB0, TC0, TD0, TE0, TF0, TG0, TH0, TI0, TJ0, TK0, TL0, TM0, TN0, TO0, TP0, TQ0, TR0, TS0, TT0, TU0, TV0, TW0, TX0, TY0, TZ0, UA0, UB0, UC0, UD0, UE0, UF0, UG0, UH0, UI0, UJ0, UK0, UL0, UM0, UN0, UO0, UP0, UQ0, UR0, US0, UT0, UV0, UW0, UX0, UY0, UZ0, VA0, VB0, VC0, VD0, VE0, VF0, VG0, VH0, VI0, VJ0, VK0, VL0, VM0, VN0, VO0, VP0, VQ0, VR0, VS0, VT0, VU0, VV0, VW0, VX0, VY0, VZ0, WA0, WB0, WC0, WD0, WE0, WF0, WG0, WH0, WI0, WJ0, WK0, WL0, WM0, WN0, WO0, WP0, WQ0, WR0, WS0, WT0, WU0, WV0, WW0, WX0, WY0, WZ0, XA0, XB0, XC0, XD0, XE0, XF0, XG0, XH0, XI0, XJ0, XK0, XL0, XM0, XN0, XO0, XP0, XQ0, XR0, XS0, XT0, XU0, XV0, XW0, XX0, XY0, XZ0, YA0, YB0, YC0, YD0, YE0, YF0, YG0, YH0, YI0, YJ0, YK0, YL0, YM0, YN0, YO0, YP0, YQ0, YR0, YS0, YT0, YU0, YV0, YW0, YX0, YY0, YZ0, ZA0, ZB0, ZC0, ZD0, ZE0, ZF0, ZG0, ZH0, ZI0, ZJ0, ZK0, ZL0, ZM0, ZN0, ZO0, ZP0, ZQ0, ZR0, ZS0, ZT0, ZU0, ZV0, ZW0, ZX0, ZY0, ZZ0.

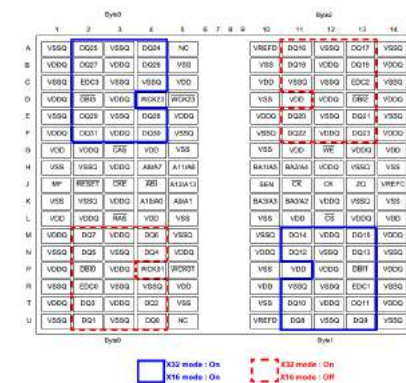
Figure 7-8. YREF-C Connections for x16 Mode



5.1 GDDR5 SRAM 170ball BGA Ball-out MF=0



5.2 GDDR5 SRAM 170ball BGA Ball-out MF=1



Signal Assignment in MF=0 and MF=1

Minor Function Signal Mapping Columns 1 to 9

A1	VSSQ	A2	DQ0	DQ23	A3	VSSQ	A4	DQ0	DQ24	A5	VSSQ	
B1	VSSQ	B2	DQ0	DQ27	B3	VSSQ	B4	DQ0	DQ28	B5	VSSQ	
C1	VSSQ	C2	DQ0	DQ31	C3	VSSQ	C4	VSSQ	DQ0	DQ35	C5	VSSQ
D1	VSSQ	D2	DQ0	DQ35	D3	VSSQ	D4	VSSQ	DQ0	DQ39	D5	VSSQ
E1	VSSQ	E2	DQ0	DQ39	E3	VSSQ	E4	VSSQ	DQ0	DQ43	E5	VSSQ
F1	VSSQ	F2	DQ0	DQ43	F3	VSSQ	F4	VSSQ	DQ0	DQ47	F5	VSSQ
G1	VSSQ	G2	DQ0	DQ47	G3	VSSQ	G4	VSSQ	DQ0	DQ51	G5	VSSQ
H1	VSSQ	H2	DQ0	DQ51	H3	VSSQ	H4	VSSQ	DQ0	DQ55	H5	VSSQ
I1	VSSQ	I2	DQ0	DQ55	I3	VSSQ	I4	VSSQ	DQ0	DQ59	I5	VSSQ
J1	VSSQ	J2	DQ0	DQ59	J3	VSSQ	J4	VSSQ	DQ0	DQ63	J5	VSSQ
K1	VSSQ	K2	DQ0	DQ63	K3	VSSQ	K4	VSSQ	DQ0	DQ67	K5	VSSQ
L1	VSSQ	L2	DQ0	DQ67	L3	VSSQ	L4	VSSQ	DQ0	DQ71	L5	VSSQ
M1	VSSQ	M2	DQ0	DQ71	M3	VSSQ	M4	VSSQ	DQ0	DQ75	M5	VSSQ
N1	VSSQ	N2	DQ0	DQ75	N3	VSSQ	N4	VSSQ	DQ0	DQ79	N5	VSSQ
O1	VSSQ	O2	DQ0	DQ79	O3	VSSQ	O4	VSSQ	DQ0	DQ83	O5	VSSQ
P1	VSSQ	P2	DQ0	DQ83	P3	VSSQ	P4	VSSQ	DQ0	DQ87	P5	VSSQ
Q1	VSSQ	Q2	DQ0	DQ87	Q3	VSSQ	Q4	VSSQ	DQ0	DQ91	Q5	VSSQ
R1	VSSQ	R2	DQ0	DQ91	R3	VSSQ	R4	VSSQ	DQ0	DQ95	R5	VSSQ
S1	VSSQ	S2	DQ0	DQ95	S3	VSSQ	S4	VSSQ	DQ0	DQ99	S5	VSSQ

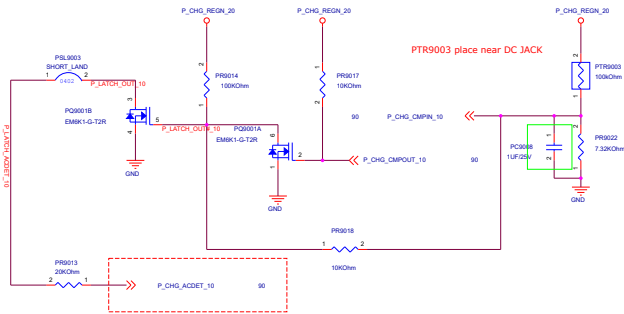
Minor Function Signal Mapping Columns 10 to 14

Pin	MF=0	MF=1	Pin	MF=0	MF=1	Pin	MF=0	MF=1	Pin	MF=0	MF=1
B10	VREFP	B11	DQ8	DQ10	B12	VSSQ	B13	DQ8	DQ11	B14	VSSQ
B15	VSSQ	B16	DQ8	DQ14	B17	VSSQ	B18	DQ8	DQ15	B19	VSSQ
C10	VSSQ	C11	DQ8	DQ18	C12	VSSQ	C13	DQ8	DQ19	C14	VSSQ
D10	VSSQ	D11	DQ8	DQ22	D12	VSSQ	D13	DQ8	DQ23	D14	VSSQ
E10	VSSQ	E11	DQ8	DQ26	E12	VSSQ	E13	DQ8	DQ27	E14	VSSQ
F10	VSSQ	F11	DQ8	DQ30	F12	VSSQ	F13	DQ8	DQ31	F14	VSSQ
G10	VSSQ	G11	DQ8	DQ34	G12	VSSQ	G13	DQ8	DQ35	G14	VSSQ
H10	VSSQ	H11	DQ8	DQ38	H12	VSSQ	H13	DQ8	DQ39	H14	VSSQ
I10	VSSQ	I11	DQ8	DQ42	I12	VSSQ	I13	DQ8	DQ43	I14	VSSQ
J10	VSSQ	J11	DQ8	DQ46	J12	VSSQ	J13	DQ8	DQ47	J14	VSSQ
K10	VSSQ	K11	DQ8	DQ50	K12	VSSQ	K13	DQ8	DQ51	K14	VSSQ
L10	VSSQ	L11	DQ8	DQ54	L12	VSSQ	L13	DQ8	DQ55	L14	VSSQ
M10	VSSQ	M11	DQ8	DQ58	M12	VSSQ	M13	DQ8	DQ59	M14	VSSQ
N10	VSSQ	N11	DQ8	DQ62	N12	VSSQ	N13	DQ8	DQ63	N14	VSSQ
O10	VSSQ	O11	DQ8	DQ66	O12	VSSQ	O13	DQ8	DQ67	O14	VSSQ
P10	VSSQ	P11	DQ8	DQ70	P12	VSSQ	P13	DQ8	DQ71	P14	VSSQ
Q10	VSSQ	Q11	DQ8	DQ74	Q12	VSSQ	Q13	DQ8	DQ75	Q14	VSSQ
R10	VSSQ	R11	DQ8	DQ78	R12	VSSQ	R13	DQ8	DQ79	R14	VSSQ
S10	VSSQ	S11	DQ8	DQ82	S12	VSSQ	S13	DQ8	DQ83	S14	VSSQ
T10	VSSQ	T11	DQ8	DQ86	T12	VSSQ	T13	DQ8	DQ87	T14	VSSQ
U10	VREFP	U11	DQ8	DQ90	U12	VSSQ	U13	DQ8	DQ91	U14	VSSQ

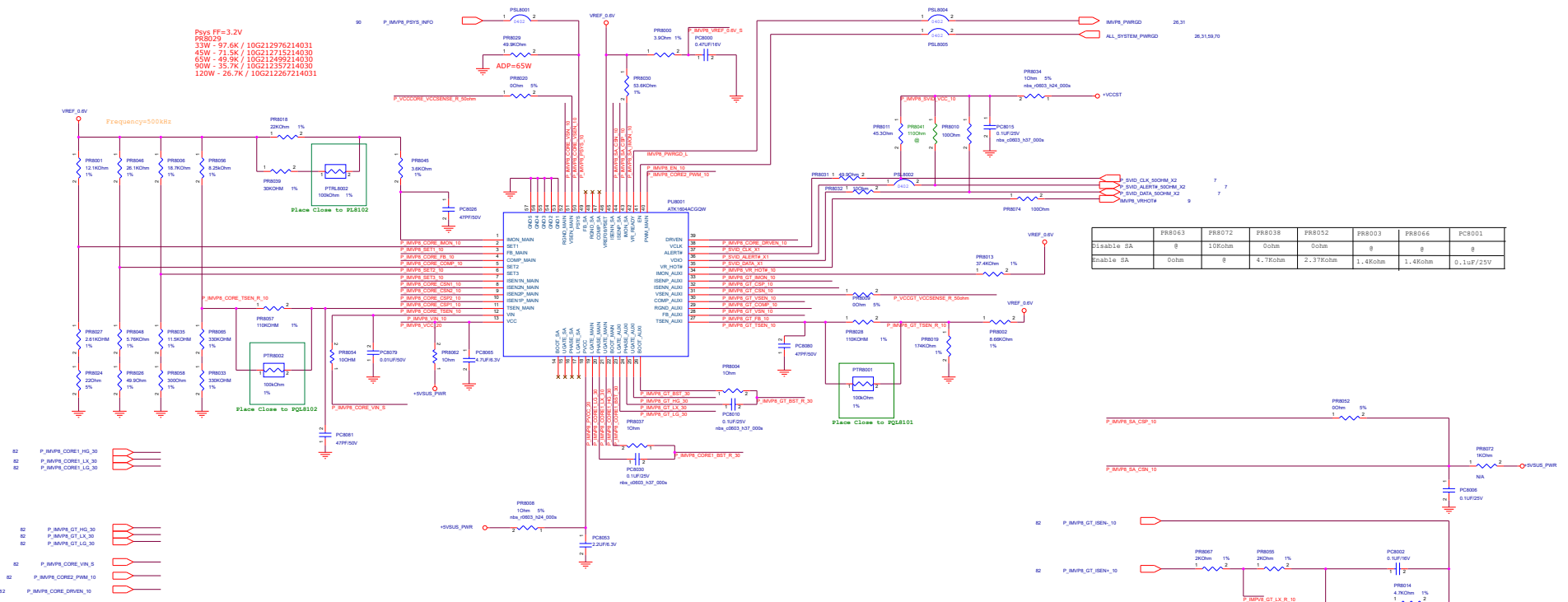
Address	0x7E	0x7C	0x7A	0x78	0x76	0x74	0x72	0x70
PR0001	10k	1.5k	2k	3.6k	3.9k	4.3k	5.2k	6k
PR0002	Open	8.2k	6.2k	6.8k	4.7k	3.6k	2.7k	2k

Address	Gx00	Gx01	Gx02	Gx03	Gx04	Gx05	Gx06
R/W	W	W	W	R	R	R	R
Function	Temp. alert threshold setting			Sensed temp. data			bit 4 = 0 bit 3 = 0 bit 6 = 0 When ALERT# assert

Address	0x7E	0x7C	0x7A	0x78	0x76	0x74	0x72	0x70
000008	10k	1.5k	2k	3.6k	3.9k	4.3k	5.1k	6k
000009	Open	8.2k	6.2k	6.8k	4.7k	3.6k	2.7k	2k

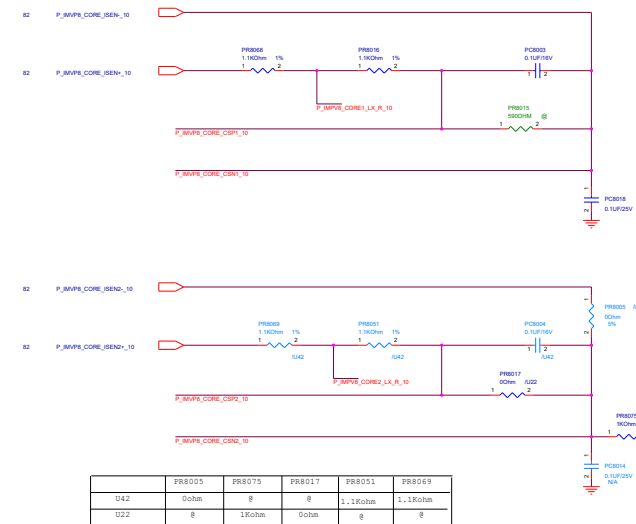
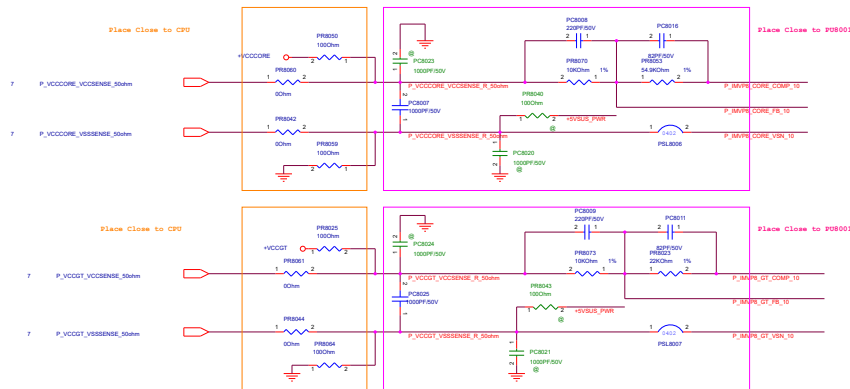


Psys FF=3.2V
 PRS020
 33W - 97.6K / 10G212976214031
 45W - 71.5K / 10G212715214030
 65W - 49.9K / 10G212495214030
 90W - 35.7K / 10G21235714030
 120W - 26.7K / 10G212267214031



	PRB063	PRB072	PRB038	PRB052	PRB003	PRB066	PCB001
Disable SA	0	10Kohm	0ohm	0ohm	0	0	0
Enable SA	0ohm	0	4.7Kohm	2.37Kohm	1.4Kohm	1.4Kohm	0.1uF/25V

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	PRB005	PRB075	PRB017	PRB051	PRB069
U42	0ohm	0	0	1.1Kohm	1.1Kohm
U22	0	1Kohm	0ohm	0	0

Title		
<Title>		
Size	Document Number	Rev
A	<Doc>	<RevCode>
Date:	Wednesday, March 07, 2018	Sheet 2 of 1

CPT
GPIO

For 555 N/A

Head Add 8C

For 555 N/A

For 555 N/A

For 555 N/A

For 555 N/A

For 555 N/A

For 555 N/A

For 555 N/A

For 555 N/A

For 555 N/A

For 555 N/A

For 555 N/A

For 555 N/A

For 555 N/A

For 555 N/A

For 555 N/A

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For 555 N/A

For 555 N/A

X5410V Change

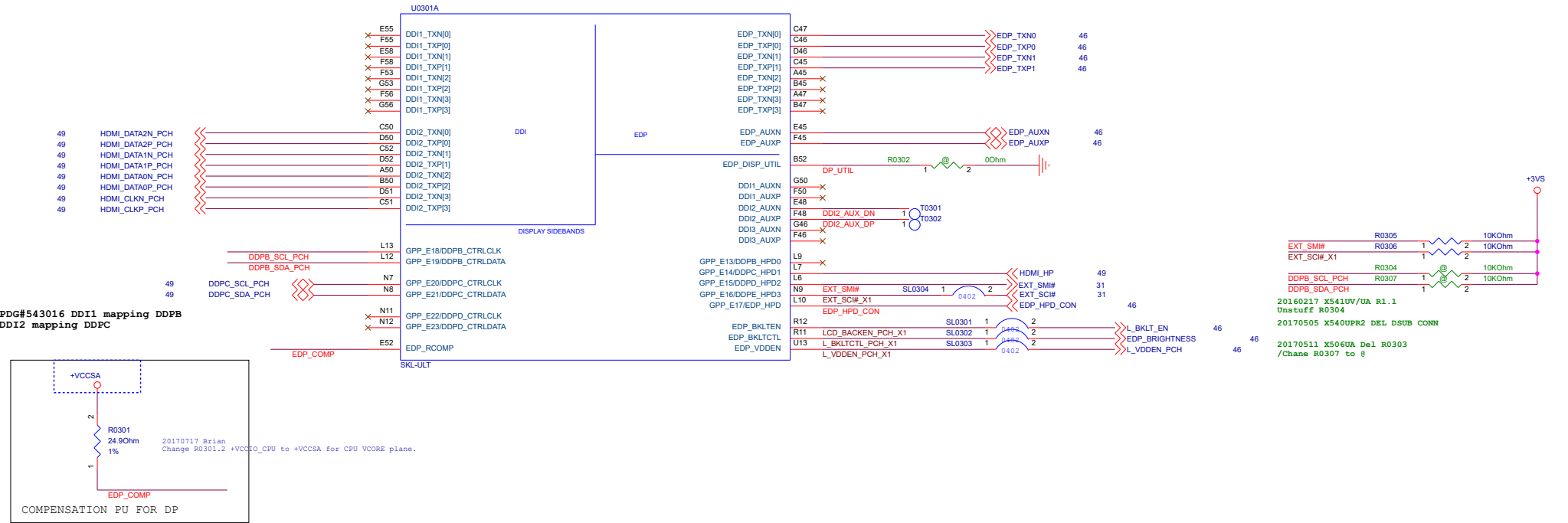
PCB_TRACE GPIO	Trace A/B	Sigmap Name	Power/Default Status	I/O/E Pin Polarity down	Power
GPP_A0	NativeW4	RC_100			
GPP_A1	NativeW4	LPC_A00			
GPP_A2	NativeW4	LPC_A01			
GPP_A3	NativeW4	LPC_A02			
GPP_A4	NativeW4	LPC_A03			
GPP_A5	NativeW4	LPC_FRAME#			
GPP_A6	NativeW4	INT_SERIAL			
GPP_A7	GPIO	N/A			
GPP_A8	NativeW4	PR_CLK300M			
GPP_A9	NativeW4	CLK_KBCPC1_PCH			
GPP_A10	NativeW4	CLK_SERIAL			
GPP_A11	GPIO	N/A			
GPP_A12	GPIO	N/A			
GPP_A13	NativeW4	GPIOB0000			
GPP_A14	NativeW4	PCR_S01_STAT#			
GPP_A15	NativeW4	PCR_S00ACEN#			
GPP_A16	GPIO	N/A (SD_LF0_SEL)			
GPP_A17	GPIO	N/A (SD_PMB_N0#)			
GPP_A18	GPIO	N/A			
GPP_A19	GPIO	N/A			
GPP_A20	GPIO	N/A			
GPP_A21	GPIO	N/A			
GPP_A22	GPIO	N/A			
GPP_A23	GPIO	N/A			
GPP_B0	NativeW4	N/A (VOC0P0M_VID0)			
GPP_B1	NativeW4	N/A (VOC0P0M_VID0)			
GPP_B2	GPIO	N/A			
GPP_B3	GPIO	N/A			
GPP_B4	GPIO	N/A			
GPP_B5	NativeW4	CR_REQ_P0#			
GPP_B6	NativeW4	CR_REQ_P1#			
GPP_B7	NativeW4	CR_REQ_P2#			
GPP_B8	NativeW4	CR_REQ_P3#			
GPP_B9	NativeW4	CR_REQ_P4#			
GPP_B10	NativeW4	CR_REQ_P5#			
GPP_B11	NativeW4	MEMV_P00EN (N/A)			
GPP_B12	NativeW4	PCR_SLP_00#			
GPP_B13	NativeW4	PLT_00#			
GPP_B14	GPIO	PCR_GPPB14			
GPP_B15	GPIO	N/A (GPPB15_CR_0#)			
GPP_B16	GPIO	N/A (GPPB15_CLK_0)			
GPP_B17	GPIO	N/A (GPPB15_M0_0)			
GPP_B18	GPIO	N/A (PCR_GPPB18)			
GPP_B19	GPIO	BF_ON/OFF#			
GPP_B20	GPIO	GPIO_V0000			
GPP_B21	GPIO	GPIO_P0_CLAMP_GPIO0			
GPP_B22	GPIO	PCR_GPPB22			
GPP_B23	NativeW4	SMGLIALEXT#			
GPP_C0	NativeW4	SMC_CR			
GPP_C1	NativeW4	SMC_DATA			
GPP_C2	GPIO	GPP_C2			
GPP_C3	GPIO	SMG2_CR			
GPP_C4	GPIO	SMG2_DATA			
GPP_C5	GPIO	GPP_C5			
GPP_C6	GPIO	SMG1_CR			
GPP_C7	GPIO	SMG1_DATA			
GPP_C8	GPIO	N/A (PCR_GPPC8)			
GPP_C9	GPIO	N/A (PCR_GPPC9)			
GPP_C10	GPIO	N/A (PCR_GPPC10)			
GPP_C11	GPIO	N/A (PCR_GPPC11)			
GPP_C12	GPIO	SDMM_SEL0			
GPP_C13	GPIO	SDMM_SEL1			
GPP_C14	GPIO	SDMM_SEL2			
GPP_C15	GPIO	FP_R0#_GPI0			
GPP_C16	GPIO	SMC0_P000EN (N/A)			
GPP_C17	GPIO	N/A (AL0_INT0#)			
GPP_C18	NativeW4	12C1_S0A_PCH_PAD			
GPP_C19	NativeW4	12C1_SCL_PCH_PAD			
GPP_C20	GPIO	SD0_P000EN			
GPP_C21	GPIO	GPIO_P000EN			
GPP_C22	GPIO	SD0_P000EN			
GPP_C23	GPIO	TP0000_INT0#			
GPP_D0	GPIO	N/A			
GPP_D1	GPIO	N/A			
GPP_D2	GPIO	N/A			
GPP_D3	GPIO	N/A			
GPP_D4	GPIO	GPI0_DMT_ADM1142 (N/A)			
GPP_D5	GPIO	SATA_ODD_P000EN			
GPP_D6	GPIO	SATA_ODD_S0A			
GPP_D7	GPIO	N/A			
GPP_D8	GPIO	N/A			
GPP_D9	GPIO	PCR_L00			
GPP_D10	GPIO	ONIC_ID			
GPP_D11	GPIO	TP000PAD_ID			
GPP_D12	GPIO	TP0000_P000EN_ID			
GPP_D13	GPIO	TP000PAD_INT0#			
GPP_D14	GPIO	WLAN_LED_0			
GPP_D15	GPIO	SM000_H00_P000EN			
GPP_D16	GPIO	FP_INT#			
GPP_D17	GPIO	N/A			
GPP_D18	GPIO	N/A			
GPP_D19	GPIO	(N/A) ONIC_CLK_PCH			
GPP_D20	GPIO	(N/A) ONIC_DATA_PCH			
GPP_D21	GPIO	N/A			
GPP_D22	GPIO	N/A			

	PCB Trace	GPIO	Signal Name	Current Status	Power/Default	Power	
	GPP_D23	GPIO	N/A				IT8995 GPIO
	GPP_E0	GPIO	SD0EXT_SERIAL_0#		EXT PD 100	+3V0	
	GPP_E1	GPIO	SATA_G00_PRINT_0#		EXT PD 100	+3V0	
	GPP_E2	GPIO	SATA_M0C18_OUT#		EXT PD 100	+3V0	
	GPP_E3	GPIO	N/A				
	GPP_E4	GPIO	SATA_DEV0LP				
	GPP_E5	GPIO	SATA_PHY0LP_DIRECT				
	GPP_E6	GPIO	SATA_DEV0LP				
	GPP_E7	GPIO	N/A				
	GPP_E8	NATIVEW4	PCR_DATA_100#		EXT PD 100	+3V0	
	GPP_E9	NATIVEW4	SDM_OC_1_24_0		EXT PD 100	+3V0D0	
	GPP_E10	GPIO	SDM_OC_3_4#		EXT PD 100	+3V0D0	
	GPP_E11	GPIO	SDM_OC_5_4#		EXT PD 100	+3V0D0	
	GPP_E12	GPIO	SDM_OC_7_4#		EXT PD 100	+3V0D0	
	GPP_E13	GPIO	N/A		EXT PD 100D	PD AC 100D 00#	
	GPP_E14	NATIVEW4	SDM1_2#		EXT PD 00	+3V0 - PD AC 00#	
	GPP_E15	GPIO	EXT_00#		EXT PD 100	+3V0	
	GPP_E16	GPIO	EXT_01#		EXT PD 100	+3V0	
	GPP_E17	NATIVEW4	EXT_02_00#			PD AC 100D 00#	
	GPP_E18	GPIO	SD0S_SCL_00#				
	GPP_E19	GPIO	SD0S_SLA_00#		EXT PD 100	+3V0	
	GPP_E20	NATIVEW4	SD0P_SCL_00#		EXT PD 2_00	+3V0 PD AC 100D 00#	
	GPP_E21	NATIVEW4	SD0P_SLA_00#		EXT PD 2_00	+3V0 PD AC 100D 00#	
	GPP_E22	GPIO	N/A				
	GPP_E23	GPIO	N/A				
	GPP_F0	GPIO	N/A				
	GPP_F1	GPIO	N/A				
	GPP_F2	GPIO	N/A				
	GPP_F3	GPIO	N/A				
	GPP_F4	GPIO	N/A				
	GPP_F5	GPIO	N/A				
	GPP_F6	GPIO	N/A				
	GPP_F7	GPIO	N/A				
	GPP_F8	GPIO	N/A				
	GPP_F9	GPIO	N/A				
	GPP_F10	GPIO	N/A				
	GPP_F11	GPIO	N/A				
	GPP_F12	GPIO	N/A				
	GPP_F13	GPIO	N/A				
	GPP_F14	GPIO	N/A				
	GPP_F15	GPIO	N/A				
	GPP_F16	GPIO	N/A				
	GPP_F17	GPIO	N/A				
	GPP_F18	GPIO	N/A				
	GPP_F19	GPIO	N/A				
	GPP_F20	GPIO	N/A				
	GPP_F21	GPIO	N/A				
	GPP_F22	GPIO	N/A				
	GPP_F23	GPIO	N/A				
555 N/A	GPP_G0	GPIO	N/A (SD00_00#)				
555 N/A	GPP_G1	GPIO	N/A (SD00_01#)				
555 N/A	GPP_G2	GPIO	N/A (SD00_02#)				
555 N/A	GPP_G3	GPIO	N/A (SD00_03#)				
555 N/A	GPP_G4	GPIO	N/A (SD00_04#)				
555 N/A	GPP_G5	GPIO	N/A (SD00_05#)				
555 N/A	GPP_G6	GPIO	N/A (SD00_06#)				
555 N/A	GPP_G7	GPIO	N/A (SD00_07#)				
555 ADD	GPD0	NATIVEW4	PR_0000#_PCH		EXT PD 0_00	+3V0_100#	
	GPD1	NATIVEW4	PR_00_0000#_PCH		EXT PD 100#	+3V0_100#	
	GPD2	GPIO	PCR_0000#		EXT PD 100	+3V0_100#	
	GPD3	NATIVEW4	PCR_0000#				
	GPD4	NATIVEW4	PCR_100#		EXT PD 100#	PD AC 00	
	GPD5	NATIVEW4	PCR_100#		EXT PD 100#	PD AC 00	
	GPD6	NATIVEW4	PR_00_0_00				
	GPD7	GPIO	NR00_00#				
555 N/A	GPD8	GPIO	N/A (000_00)		EXT PD 00		
	GPD9	GPIO	PCR_00_00_00# (N/A)				
	GPD10	GPIO	PCR_00_00_00#				
	GPD11	GPIO	NR00_000# (N/A)				

Display Port

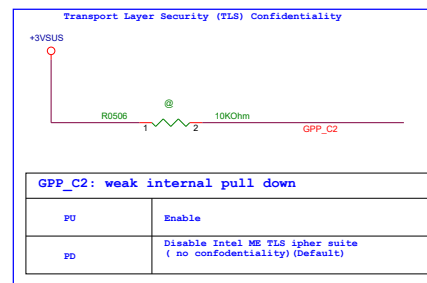
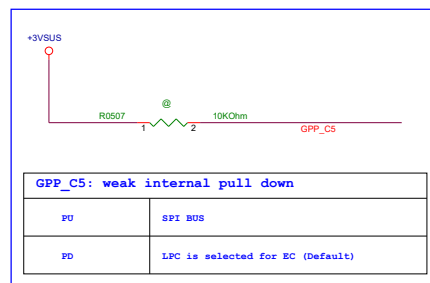
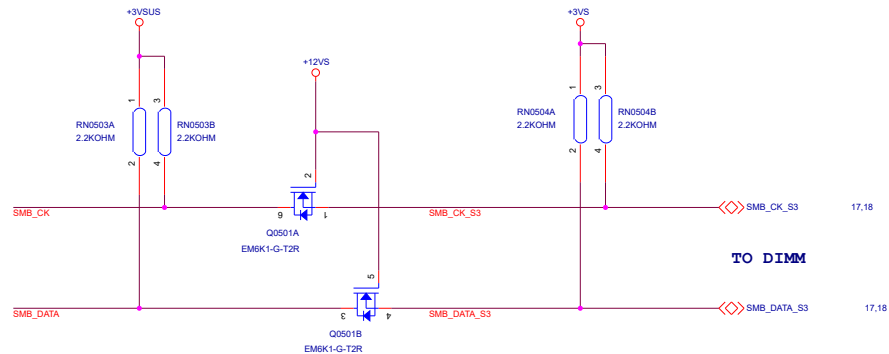
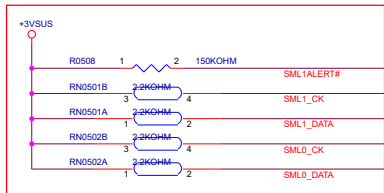
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B	
C	HDMI

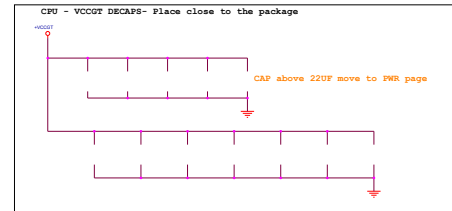
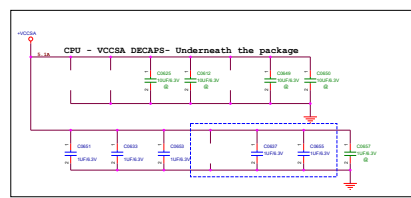
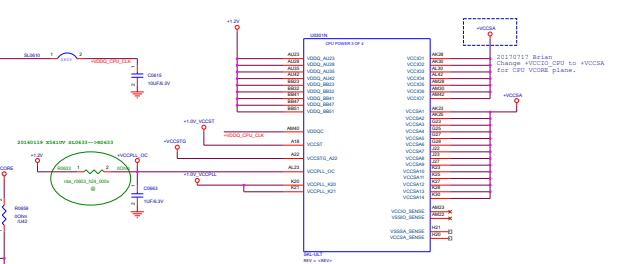
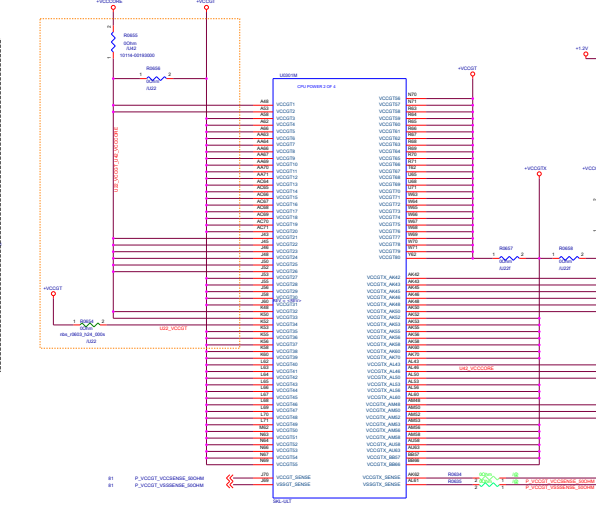
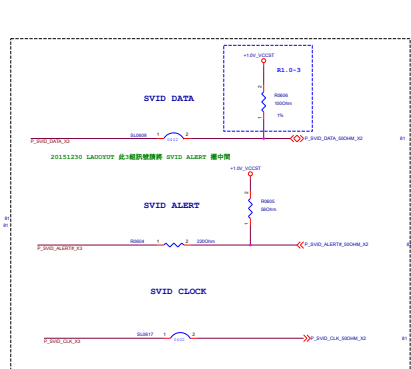
Intel Version	ASUS P/N




BOM

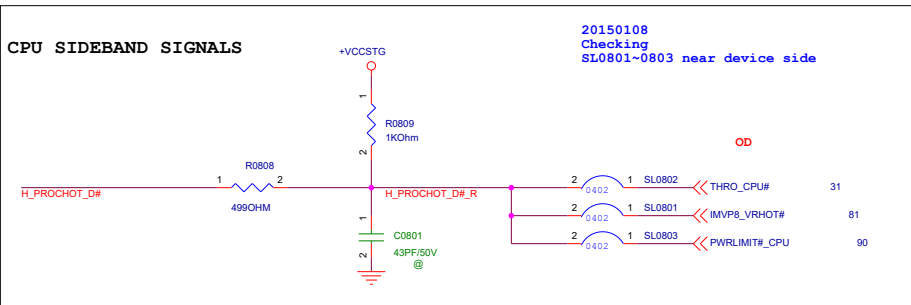
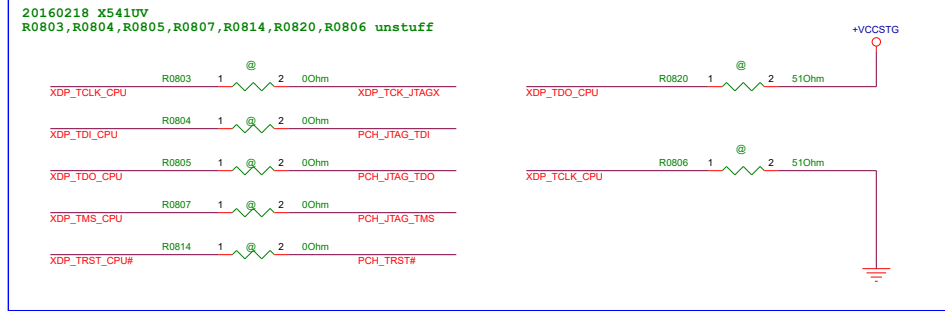
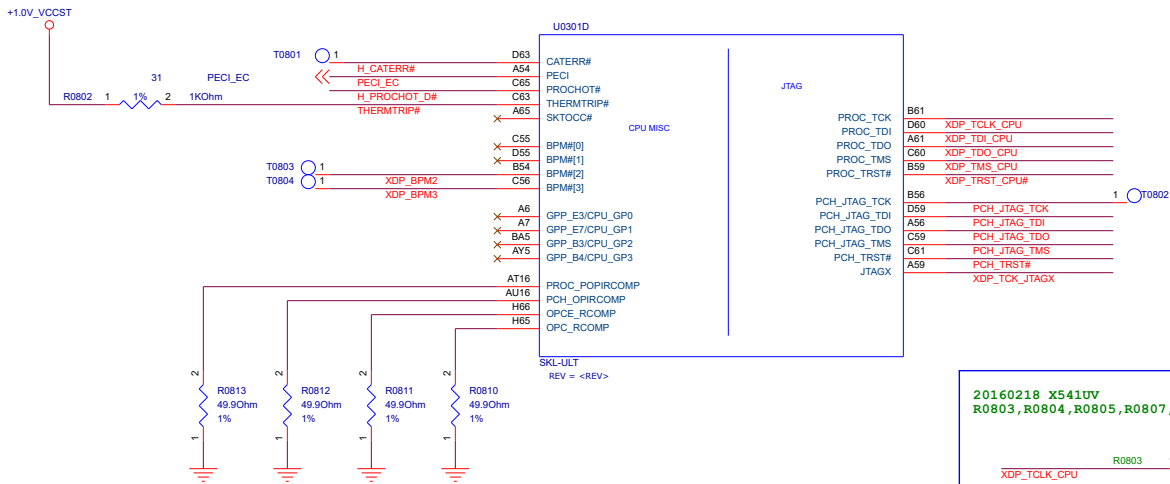
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X407UA/UV			R1.0
Title : CPU_DISPLAY			
Size Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: Brian Chen	
Date: Wednesday, March 07, 2018	Sheet	4	of 102





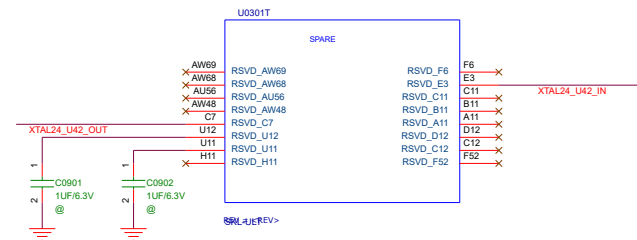
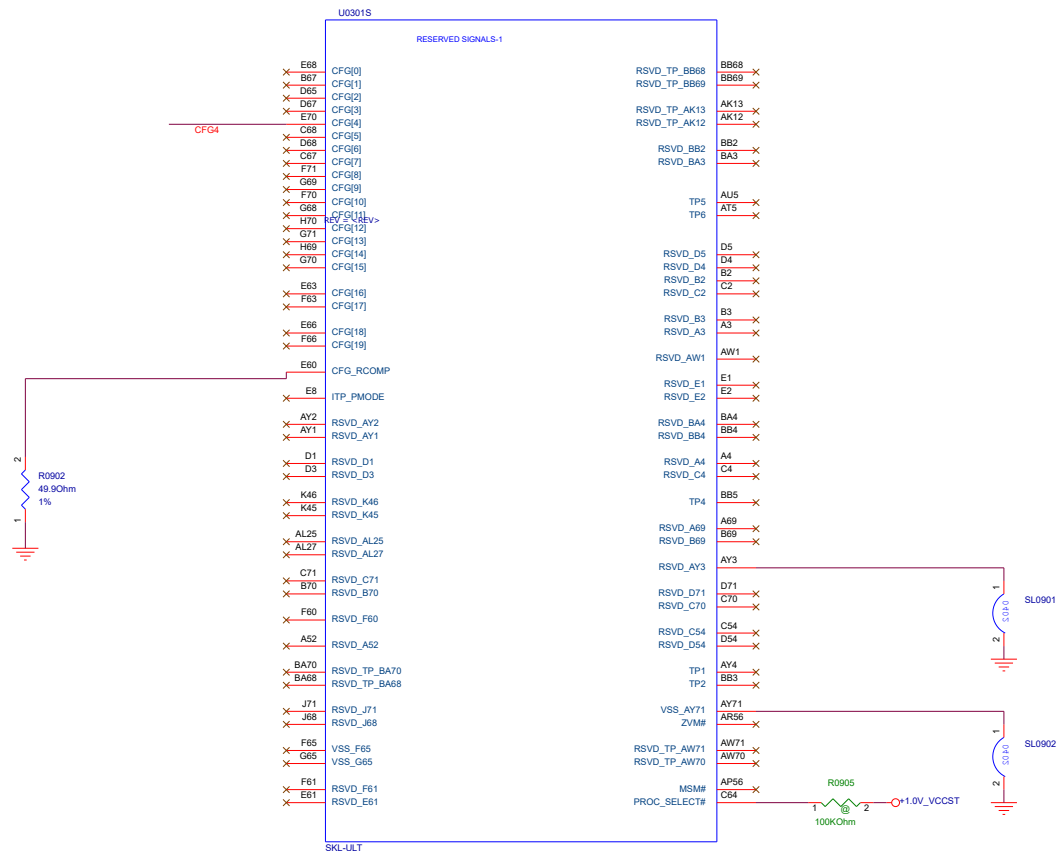
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Title : CPU_XDP		X407UA/UV	R1.0
Size	Dept.: ASUSTek COMPUTER INC. Engineer: Brian Chen		
C	Date: Wednesday, March 07, 2018		
		Sheet	8 of 102

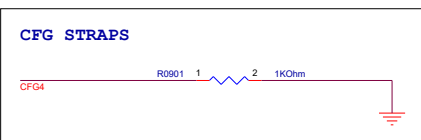
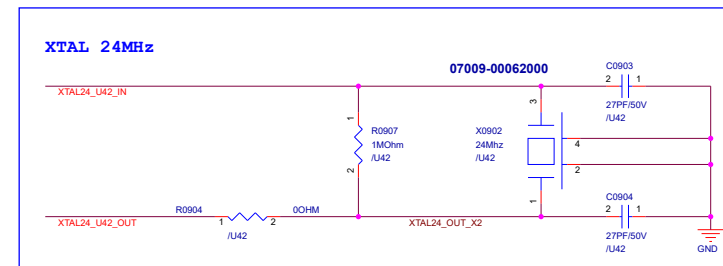


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ASUS		Project Name	Rev
		X407UA/UV	R1.0
Title : CPU_MISC,JTAG,CLK			
Size	Dept.:	ASUSTek COMPUTER INC.	Engineer: Brian Chen
B	Date: Wednesday, March 07, 2018	Sheet	9 of 102

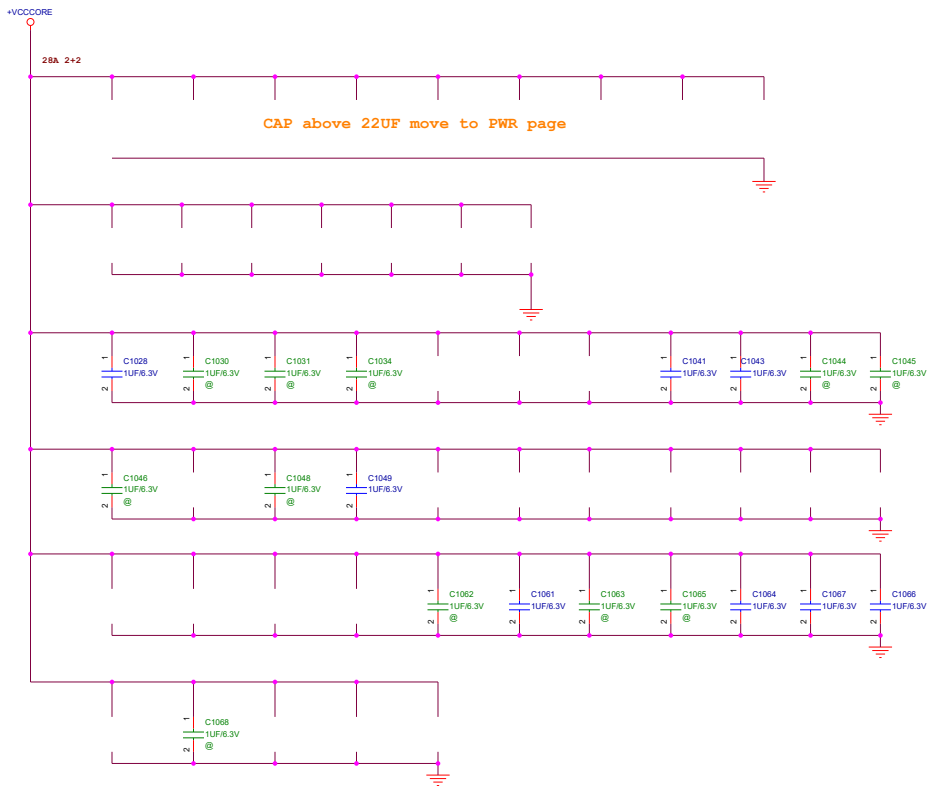


20171023 Jack Add XTAL 24M for KBL-R.

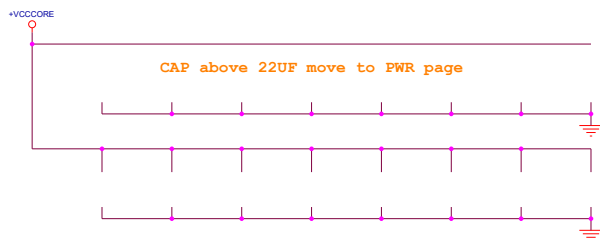


	1	0	NOTE
CFG0	NO STALL	STALL	STALL RESET SEQUENCE AFTER PCU PLL LOCK UNTIL DE-ASSERTED
CFG4	DISABLE	ENABLE	eDP ENABLE

CPU - VCC DECAPS- Underneath the package




CPU - VCC DECAPS- Place close to the package



BOM

ASUS		Project Name	Rev
X407UA/UV			R1.0
Title : CPU_POWER_CAP			
Size	Dept.:	ASUSTek COMPUTER INC.	Engineer: Brian Chen
C	Date: Wednesday, March 07, 2018	Sheet	11 of 102

		Project Name		Rev
		X407UA/UV		R1.0
Title :				
Size D	Dept.: ASUSTeK COMPUTER INC. Engineer: Brian Chen			
Date: Wednesday, March 07, 2018			Sheet	12 of 102


		Project Name		www.teknisi-indonesia.com		Rev	
				X407UA/UV		R1.0	
Title :							
Size		Dept.: ASUSTeK COMPUTER INC. Engineer:					
C							
Date: Wednesday, March 07, 2018				Sheet		13 of 102	


Table 4-2. System Memory Interface Guideline Terminology and Descriptions


SKL Processor and Memory Type	SKL H			
	DDR4/-RS SO-DIMM+ECC	DDR4/-RS SO-DIMM no ECC	DDR4/-RS Memory Down	LPDDR3 Memory Down
Signal Group Details				
Clock (CLK)	CKN[3:0], CKP[3:0]	CKN[3:0], CKP[3:0]	CKN[1:0], CKP[1:0]	CKP[1:0], CKN[1:0]
Control (CTRL)	CS#[3:0], ODT[3:0]	CS#[3:0], ODT[3:0]	CS#[1:0], ODT[1:0]	CS#[1:0], ODT[0]
Clock Enable (CKE)	CKE[3:0]	CKE[3:0]	CKE[1:0]	CKE[3:0]
Command (CMD)	MA[16:0], BG[1:0], BA[1:0], ACT#, PAR	MA[16:0], BG[1:0], BA[1:0],ACT#, PAR	MA[16:0], BG[1:0], BA[1:0], ACT#, PAR	CAA[9:0], CAB[9:0]
Strobe	DQSP[7:0], DQSN[7:0]	DQSP[7:0], DQSN[7:0]	DQSP[7:0], DQSN[7:0]	DQS[7:0], DQS#[7:0]
ECC strobe	DQSP[8], DQSN[8]	N/A	N/A	N/A
Data	DQ[63:0]	DQ[63:0]	DQ[63:0]	DQ[63:0]
ECC Data	DQ[71:64]	N/A	N/A	N/A
Alert	ALERT#	ALERT#	ALERT#	N/A
Reset	DRAM_RESET#	DRAM_RESET#	DRAM_RESET#	N/A
RCOMP	DDR_RCOMP[2:0]	DDR_RCOMP[2:0]	DDR_RCOMP[2:0]	DDR_RCOMP[2:0]

<Variant Name>

		Title : DDR4_TERMINATION_A	
		Engineer: Brian Chen	
Size C	Project Name X407UA/UV		Rev R1.0
Date: Wednesday, March 07, 2018	Sheet	14	of 102


<Variant Name>


		Title : DDR4_ON-BOARD_A_L32	
		Engineer: Brian Chen	
Size C	Project Name X407UA/UV		Rev R1.0
Date: Wednesday, March 07, 2018		Sheet 15	of 102

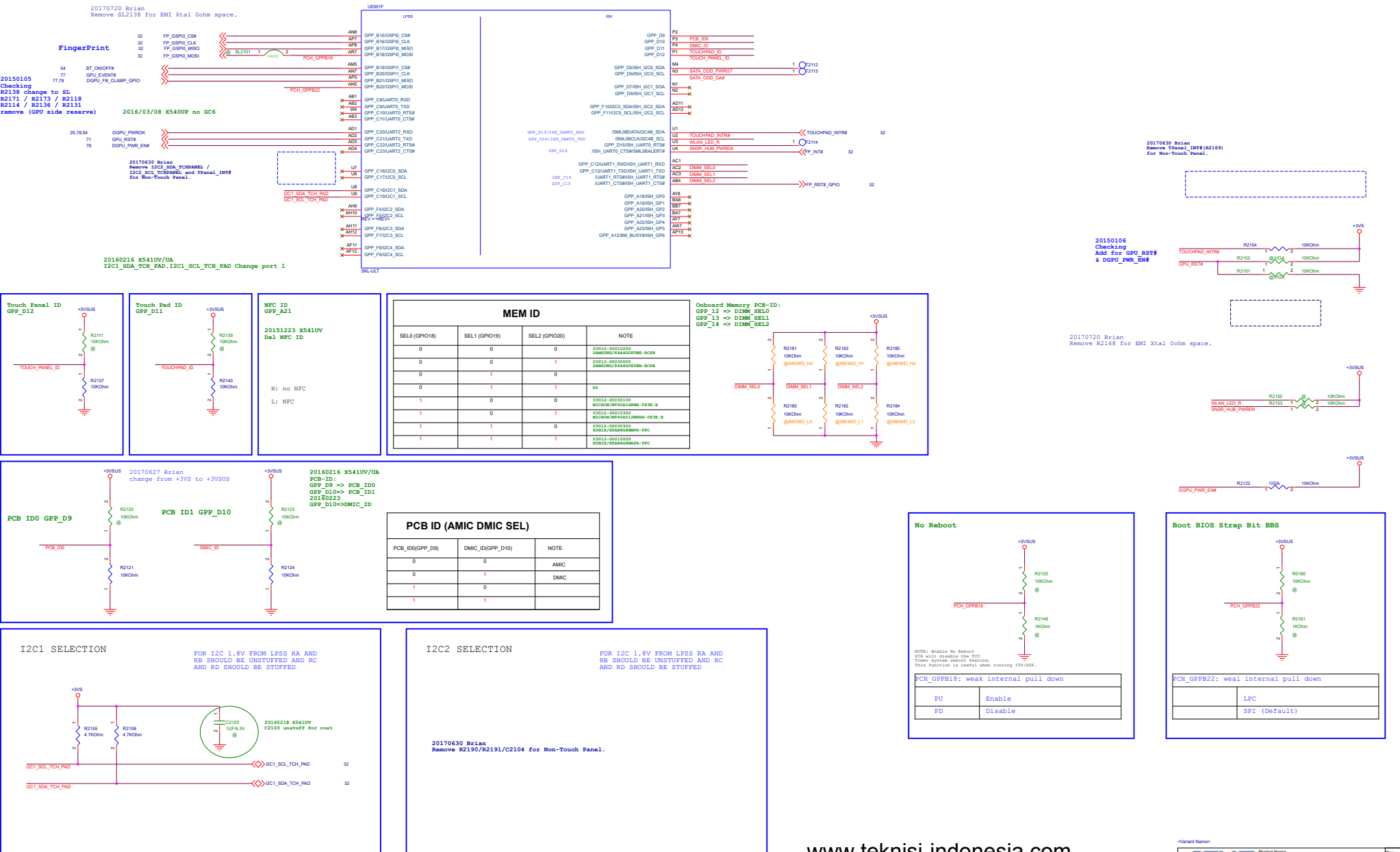
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		Engineer: Brian Chen	
Size	Project Name		Rev
C	X407UA/UV		R1.0
Date:	Wednesday, March 07, 2018	Sheet	16 of 102



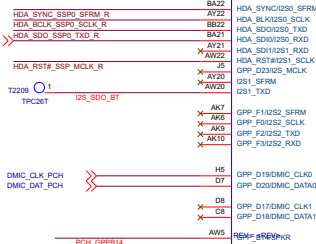
EVENT# ON ECC DIMM: KEEP A PULL UP IF NO PIN IN PCH

		Project Name		Rev
		X407UA/UV		R1.0
Title :				
Size				
C	Dept.: ASUSTeK COMPUTER INC.		Engineer:	Brian Chen
Date: Wednesday, March 07, 2018			Sheet	20 of 102

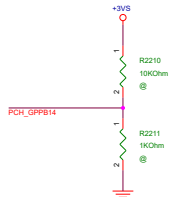
		Project Name X407UA/UV		Rev R1.0	
Title : CPU_PCH_CSI2,EMMC					
Size B		Dept.: ASUSTek COMPUTER INC.		Engineer: Brian Chen	
Date: Wednesday, March 07, 2018			Sheet 21 of 102		



RN2201 near PCH

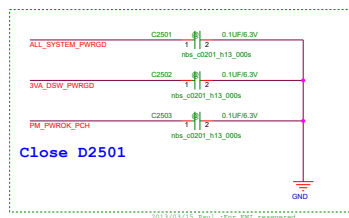
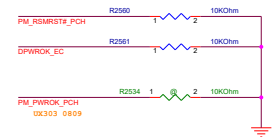
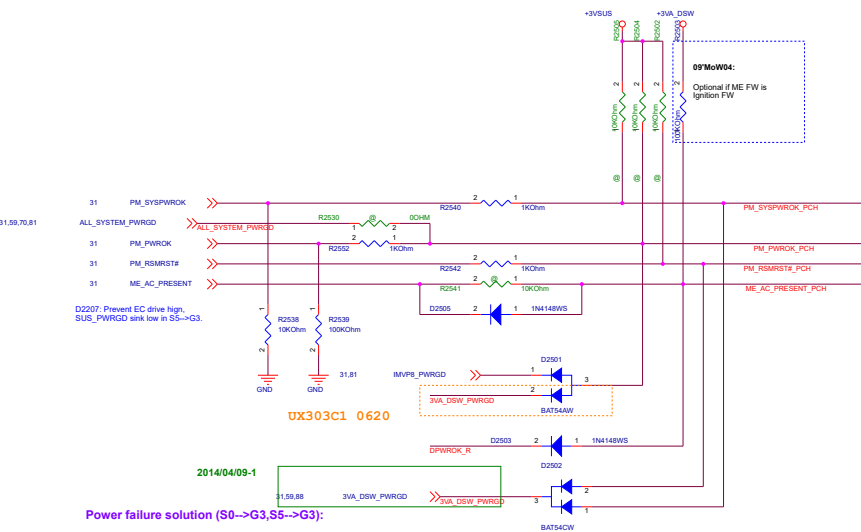
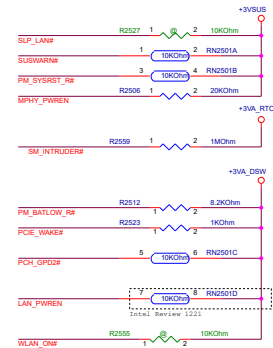
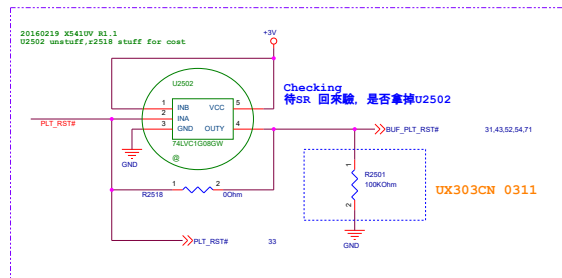
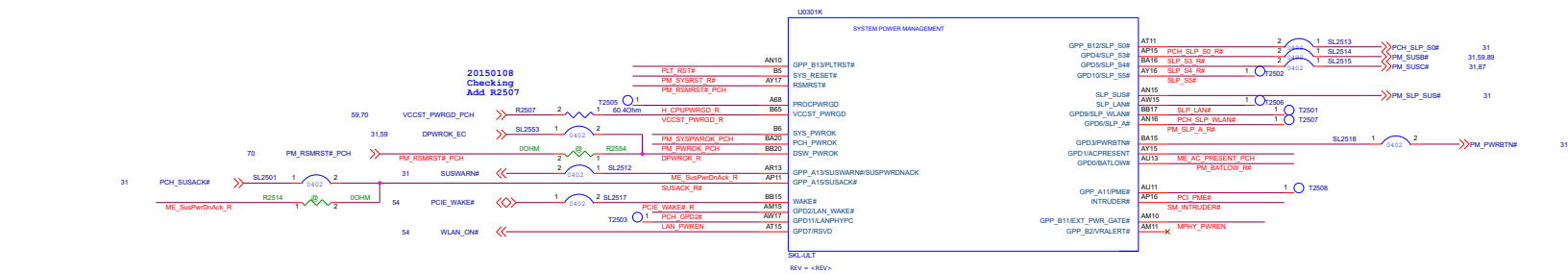


ACZ_SDOUT is a signal used for Flash
Descriptor security Override/ME debug mode
HIGH : get overrideen, LOW : disable override

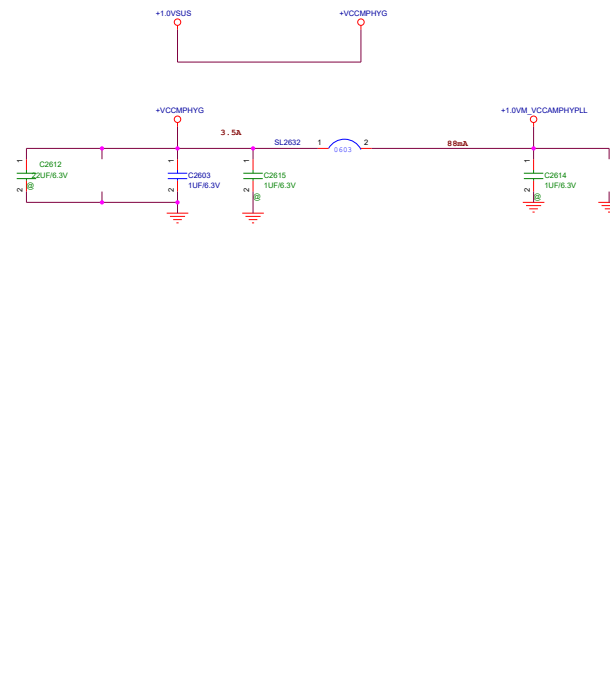
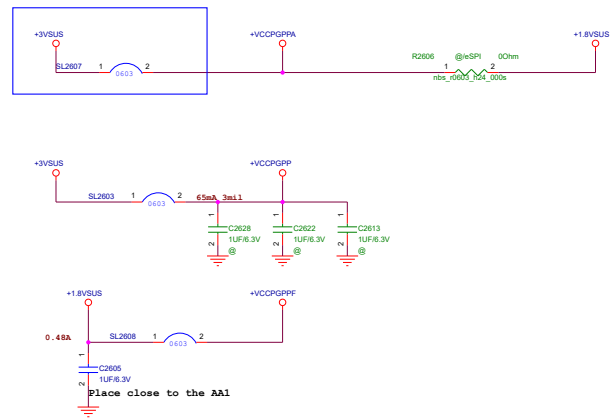


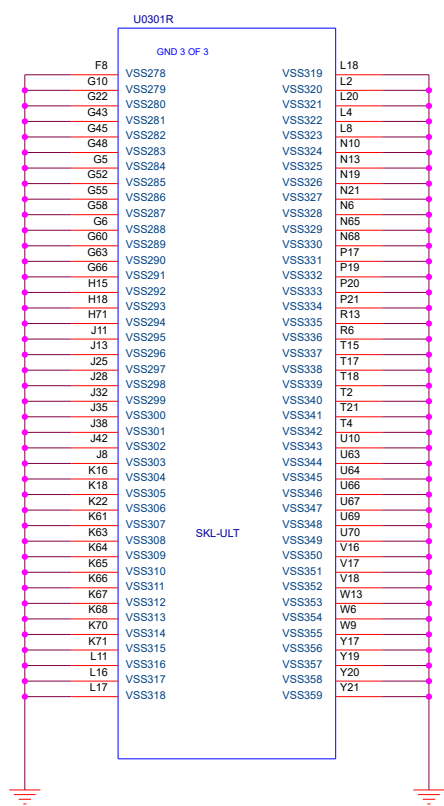
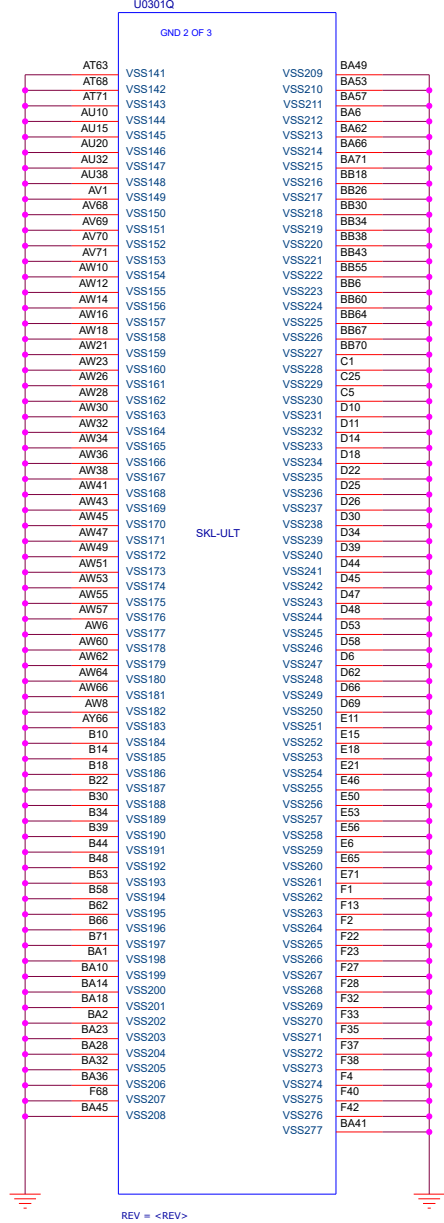
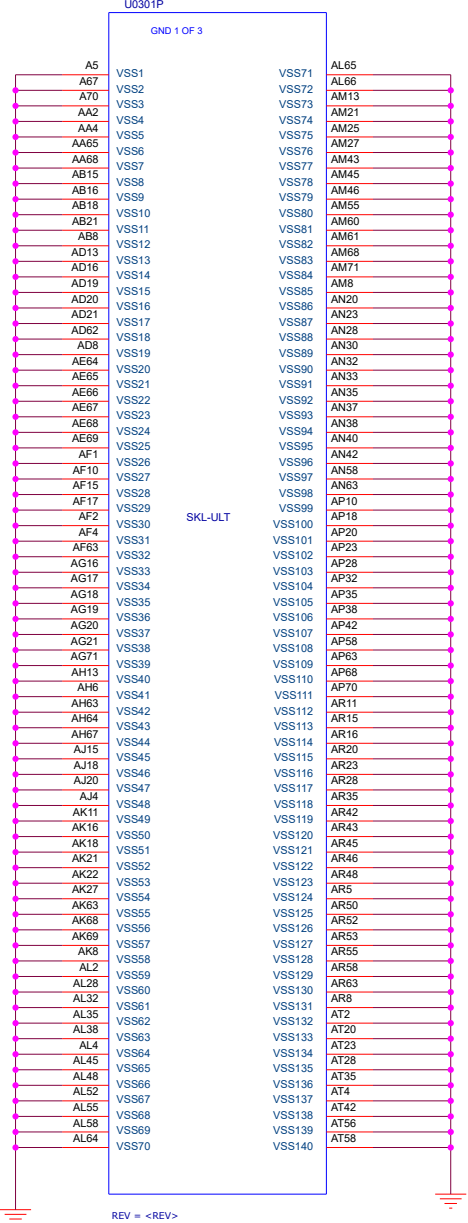
```
PCH GPPB14: weak internal pull down
```

PU	Enable
PD	Disable (default)




2017/05/12 remove R2505 ,power sequence will be check

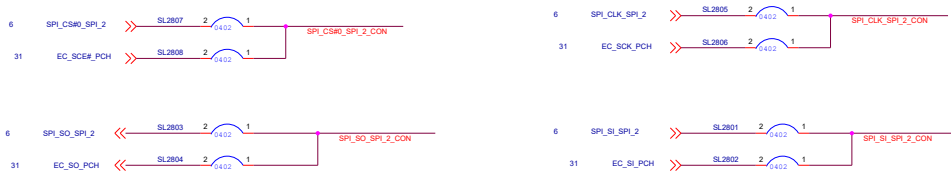




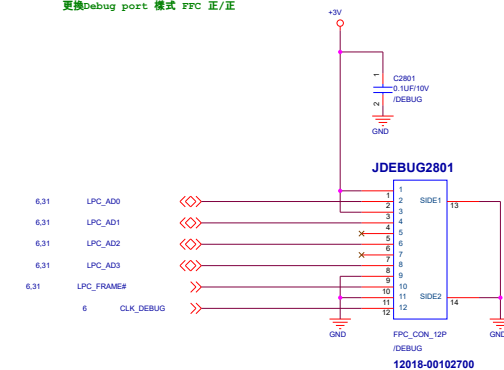
BOM

REV				Project Name		Rev
	X407UA/UV					R1.0
Title : CPU_PCH_POEWR,GND						
Size		Dept.:		ASUSTek COMPUTER INC.		Engineer:
B				Brian Chen		
Date: Wednesday, March 07, 2018				Sheet	28	of 102

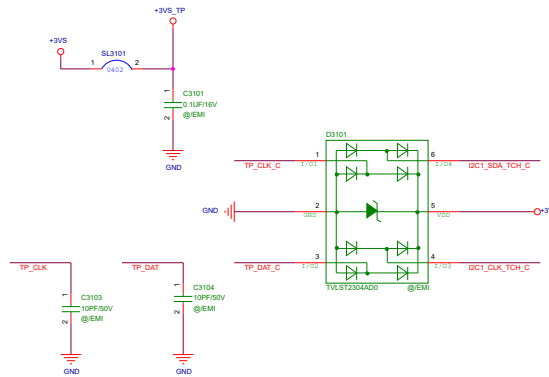
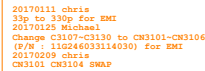
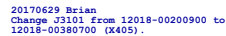
The diagram shows a circuit where a +3V_{SUS} supply is connected through a 3V_A source and a 0Ω resistor (R2809) to a Zener diode (DZ801). The Zener diode's cathode is connected to ground, and its anode is connected to a node labeled DZ801_PN12. This node is also connected to a 0Ω resistor (R2811) which leads to the +3V_{SUS_SPH} output. A note indicates the output voltage is 20160218 X541UV, DZ801unstarf, and R2811 stuff for cost.

[illegible][illegible]

```
20151225
12G183301208-->12018-00102700
更換Debug port 樣式 FFC 正/正
```



Touch PAD



	F	I
	PIN NO.	PIN DEFINITION
	1	VDD_3.3V
	2	NC
	3	D-
	4	D+
	5	GND
	6	I2C_DATA
	7	I2C_CLK
	8	TOUCH - INT

Print

2017/01/23 X5420A_R1.1 #17, FP_Power modify from +3VS to +3VS05

2017/01/23 X5420A_R1.1 #18, Remove reserve RES and add current for RST#

2016/10/20 X5420A_R1.0 #51, Add J3103 for Fingerprint

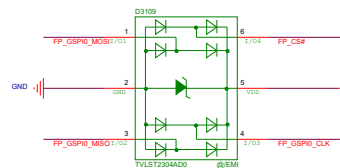
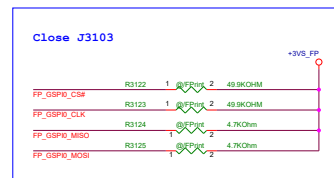
2017/02/16 X5420A_R1.1 #52, Add R3120 for FP_RST#



2017/01/23 X5420A_R1.1 #17, FP_Power modify from +3VS to +3VS05

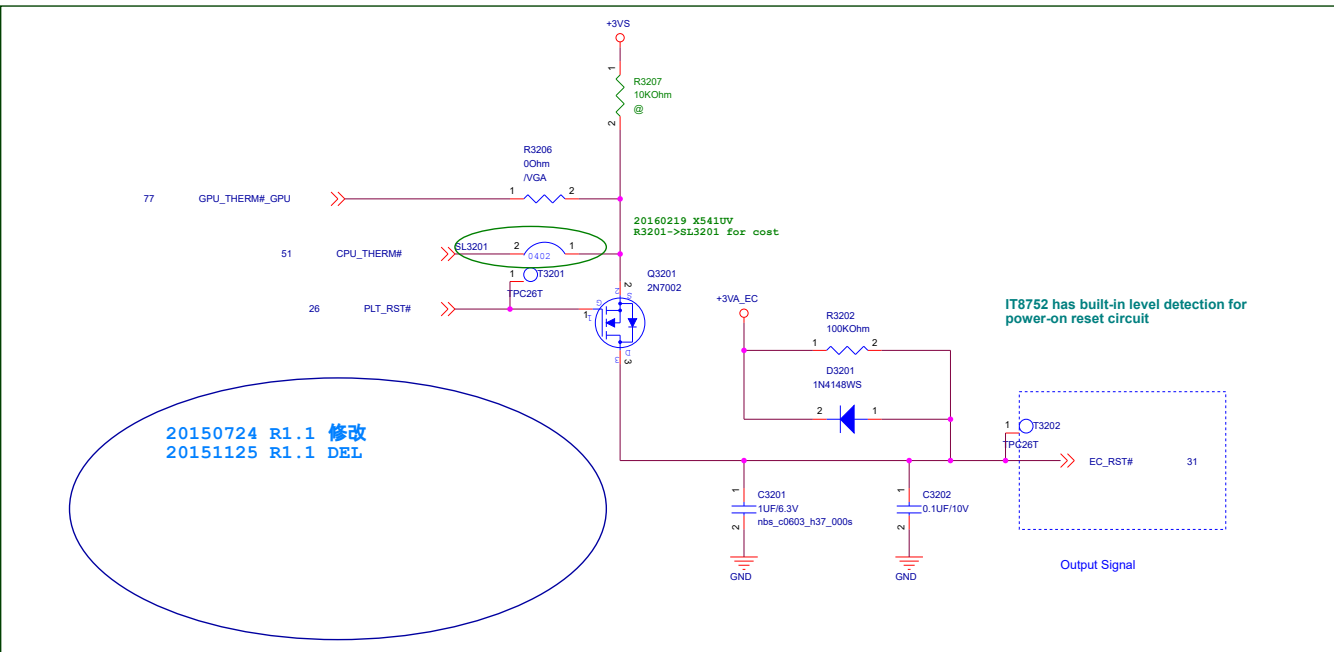
2017/01/23 X5420A_R1.1 #18, Remove reserve RES and add current for RST#

2016/10/20 X5420A_R1.0 #51, Add J3103 for Fingerprint

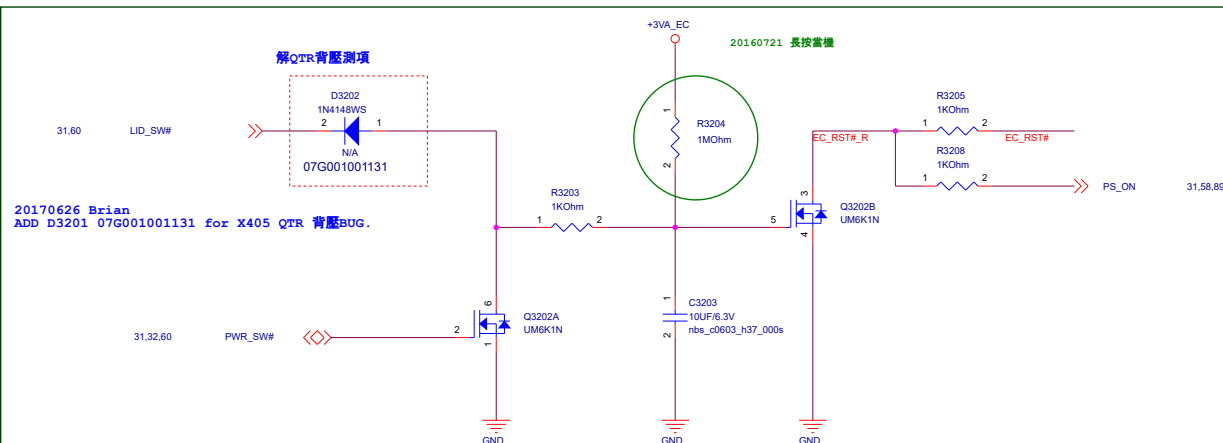
2017/02/16 X5420A_R1.1 #52, Add R3120 for FP_RST#



F		I	F		I
 CN1			 CN2		
PIN NO.	PIN DEFINE*		PIN NO.	PIN DEFINE*	
1	VDD_3.3V_TP		1	VDD_3.3V_FP	
2	GND		2	FP_RSTN	
3	PS2_CLK		3	FP_MOSI	
4	PS2_DATA		4	FP_INTN	
5	GND		5	FP_MISO	
6	SDA		6	FP_CSN	
7	SCL		7	FP_SCK	
8	INT		8	GND	

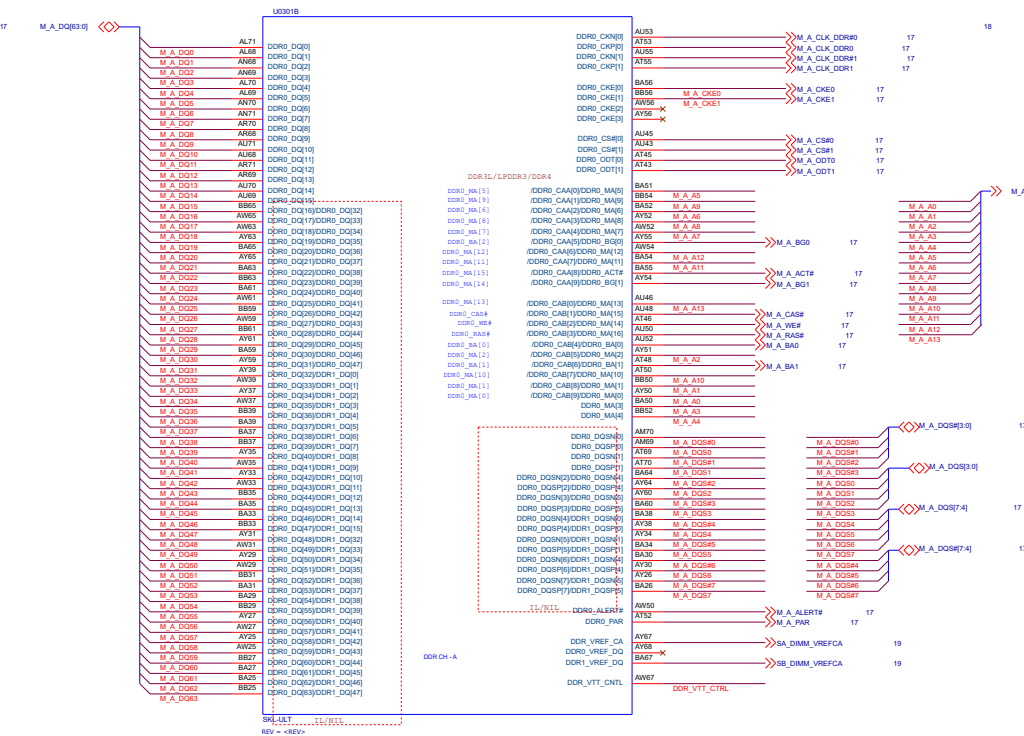



battery embedded (press pwr_sw 10sec, then reset ec)





<Variant Name>

For SO-DIMM (A)



		Project Name		Rev
		X407UA/UV		R1.0
Title : RTL8402 (LAN+CR)				
Size D	Dept.: ASUSTeK COMPUTER INC. Engineer: Brian Chen			
Date: Wednesday, March 07, 2018			Sheet	34 of 102

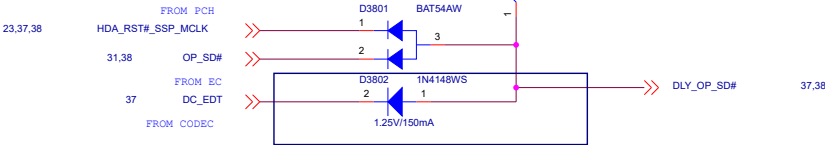
		Project Name		Rev
		X407UA/UV		R1.0
Title : RTL8402_RJ45				
Size C	Dept.: ASUSTeK COMPUTER INC. Engineer: Brian Chen			
Date: Wednesday, March 07, 2018			Sheet	35 of 102

		Project Name		Rev
		X407UA/UV		R1.0
Title :				
Size				
C	Dept.: ASUSTeK COMPUTER INC.		Engineer:	Brian Chen
Date: Wednesday, March 07, 2018			Sheet	36 of 102

20160530
1. Del R3833 & Add D3801
2. AUD_DVDD_IO--->AUD_DVDD

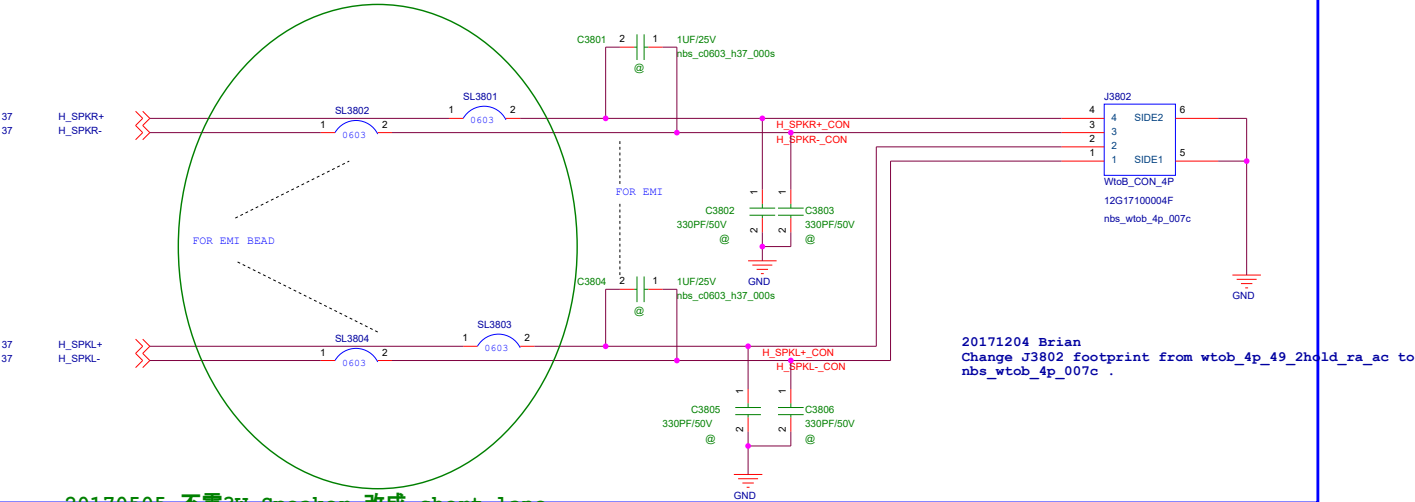
MUTE CONTROL

20151216
HDA_RST#_SSP_MCLK 由PCH 發出 (主要控制訊號)
OP_SD 由 Ec發出 (For project)



20171020 Brian
Change R3833 to D3802 for De-pop.

Trace width for
H_SPKL+ O/H SPKL- O/H SPKR+ O/H SPKR- OSpeaker
Speaker : 4 ohm : 40mil ; 8 ohm : 20mil





20171204 Brian
Change J3802 footprint from wtob_4p_49_2hold_ra_ac to
nbs_wtob_4p_007c .


20170505 不需3W Speaker 改成 short lane

BOM

ASUS		Project Name	Rev
		X407UA/UV	R1.0
Title : HDD Board-Speaker			
Size C	Dept.:	ASUSTek COMPUTER INC. Engineer:	Brian Chen
Date:	Wednesday, March 07, 2018	Sheet	39 of 102

		Project Name		Rev
		X407UA/UV		R1.0
Title : HDD Board_HDD Conn_FPC				
Size				
C	Dept.: ASUSTeK COMPUTER INC.		Engineer: Brian Chen	
Date: Wednesday, March 07, 2018			Sheet	40 of 102

		Project Name		Rev
		X407UA/UV		R1.0
Title : SDIO_CR				
Size A	Dept.: ASUSTeK COMPUTER INC. Engineer: Brian Chen			
Date: Wednesday, March 07, 2018			Sheet	41 of 102

		Project Name		Rev
		X407UA/UV		R1.0
Title : CB-****				
Size C	Dept.: ASUSTeK COMPUTER INC. Engineer: Brian Chen			
Date: Wednesday, March 07, 2018			Sheet	42 of 102

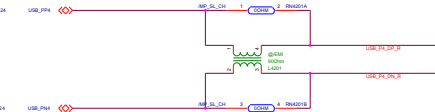
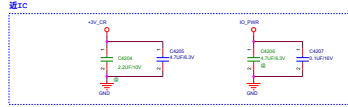
AU6465

	mode	Vin(V)	Iin (mA)	mW
AU4465 (Enable Power saving mode)	Suspend with card	3.3V	0.33	1.1
	Suspend without card	3.3V	0.14	0.46
	Idle with card	3.3V	32.8	108.24
	Idle without card	3.3V	0.14	0.46
	operating	3.3V	119	392.7

Use SanDisk SDHC 8G card (Extreme Pro)



20170322 Brian
Change ECMF(U5505U5506U5204U6603U6604U6605U5701)
to Common mode Choke coil coil.



20160906 chris
add c6659~c6662
for EMI

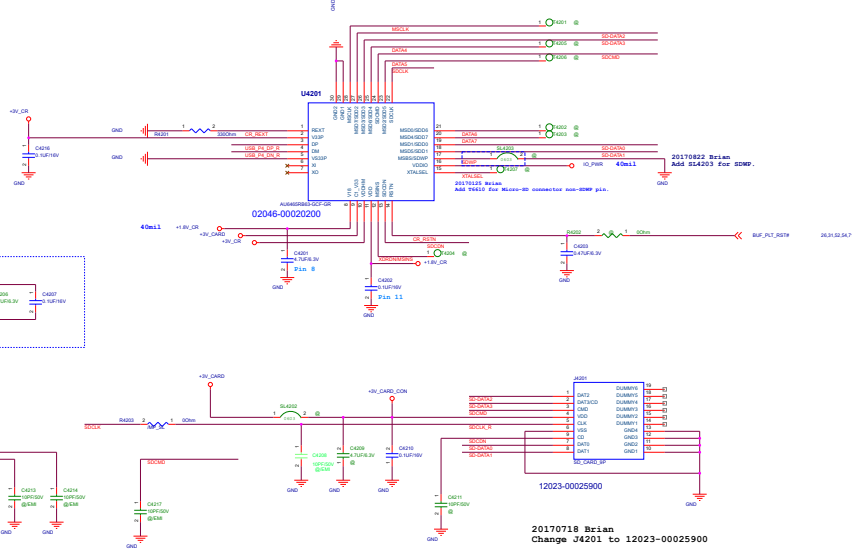


Figure 4-51. SKL U DDR4/-RS x8 Devices Memory Down V_{REF-CA} Overview

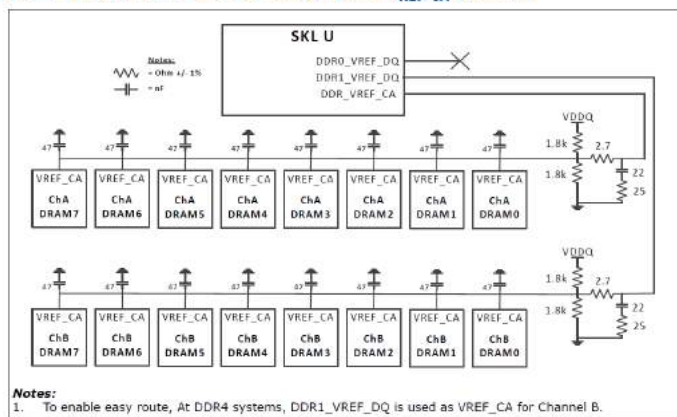
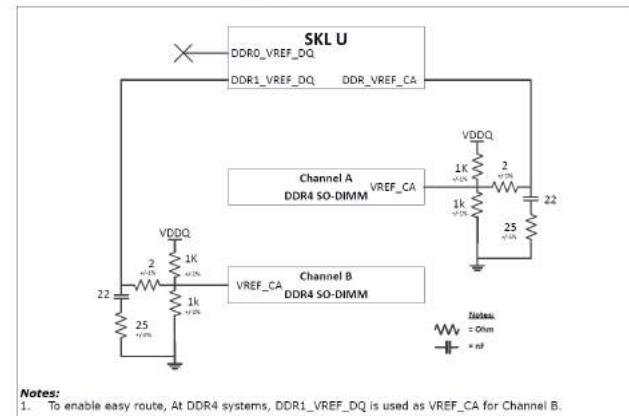
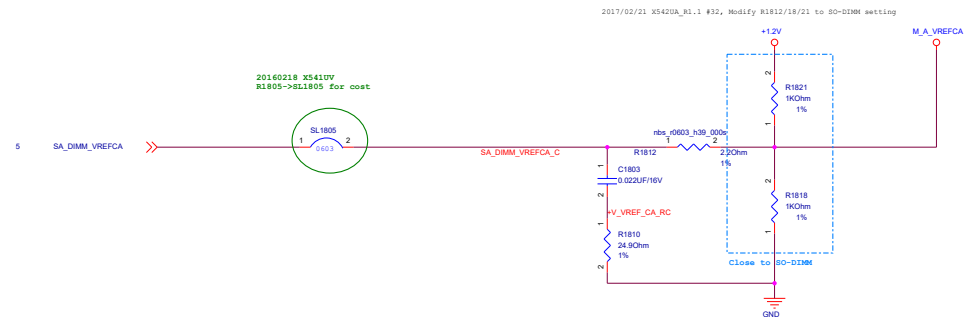
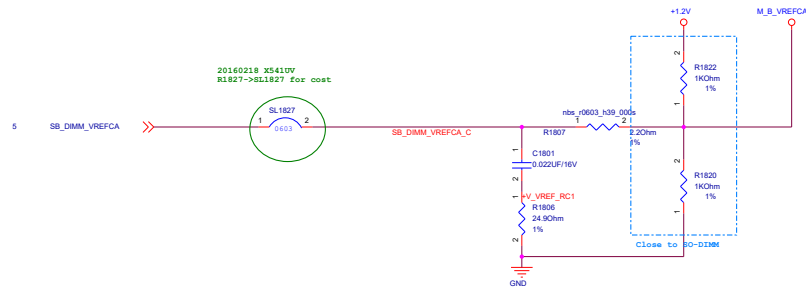


Figure 4-49. SKL U DDR4/-RS SODIMM V_{REF-CA} Overview




www.teknisi-indonesia.com


All Vref trace must be 20 mils width

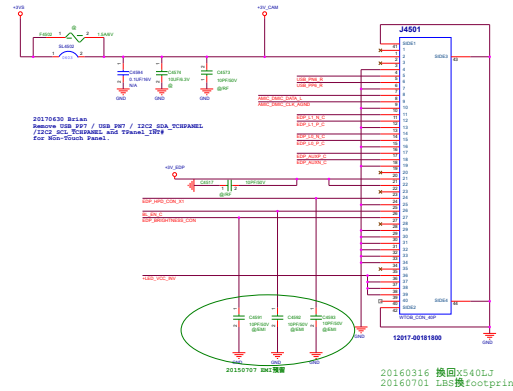
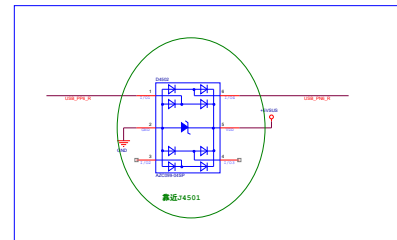
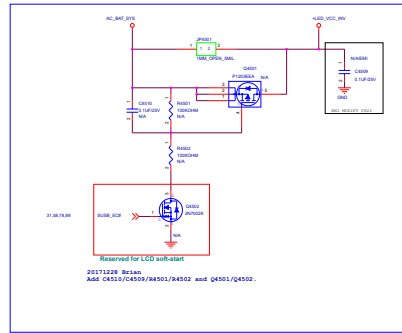
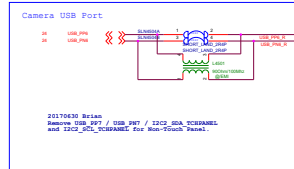
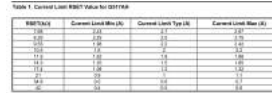


<Variant Name>


		Project Name		Rev
		X407UA/UV		R1.0
Title : CB-****				
Size C	Dept.: ASUSTeK COMPUTER INC. Engineer: Brian Chen			
Date: Wednesday, March 07, 2018			Sheet	44 of 102


BOM

		Project Name	Rev
		X407UA/UV	R1.0
Title : DEBUG PORT			
Size	Dept.: ASUSTeK COMPUTER INC. Engineer: Brian Chen		
A			
Date: Wednesday, March 07, 2018			Sheet 45 of 102



BOM

		Project Name	Rev
		X407UA/UV	R1.0
Title : LVDS CONNECTOR			
Size	Dept.: ASUSTek COMPUTER INC. Engineer: Brian Chen		
C			
Date: Wednesday, March 07, 2018	Sheet	47	of 102

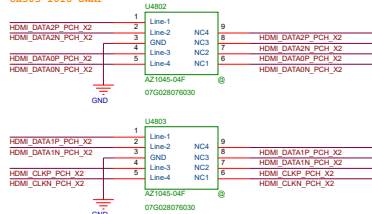
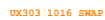
		Project Name		Rev	
		X407UA/UV		R1.0	
Title : CRT D-SUB					
Size D		Dept.: ASUSTeK COMPUTER INC. Engineer: Brian Chen			
Date: Wednesday, March 07, 2018			Sheet 48 of 102		


Near CON J4801



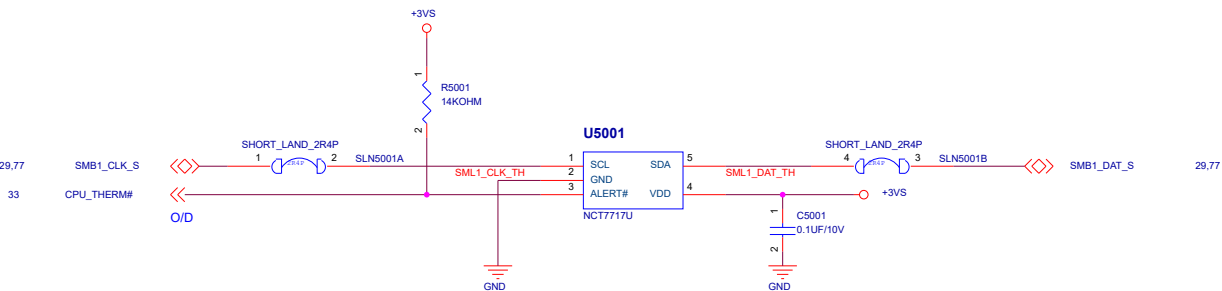
20170629 Brian
Change J4801 from 12022-00094900 to
12022-00094400(X507) .

對Pin Define

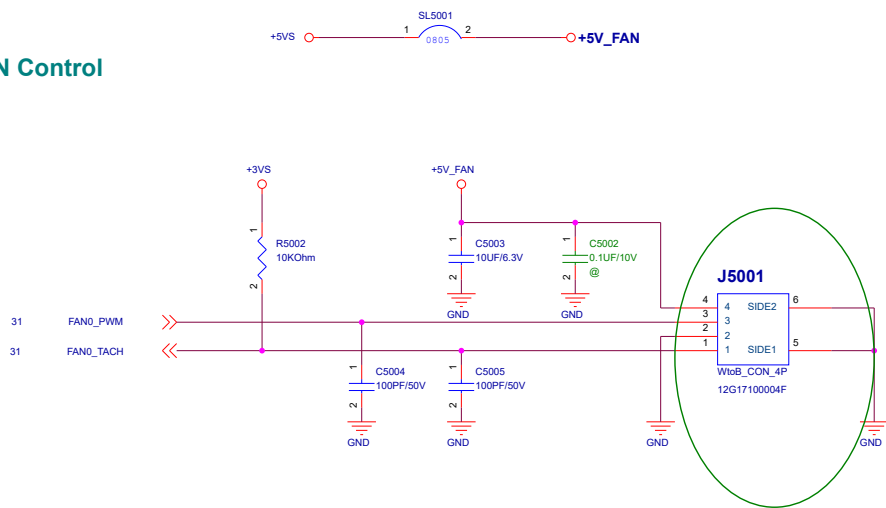


		Project Name		Rev
		X407UA/UV		R1.0
Title : TV_****				
Size	Dept.: ASUSTeK COMPUTER INC. Engineer: Brian Chen			
C				
Date: Wednesday, March 07, 2018			Sheet	50 of 102

CPU Thermal Sensor



DC FAN Control



20160316 换回X540LJ

5.3 Address Setting

NCT7717U I2C/SMBus address is 1001000xb (x is R/W bit).

5.6 ALERT# point hardware power-on setting (TBD)

The default value could be set after power up 100ms by different pull-up resistor of ALERT# pin :

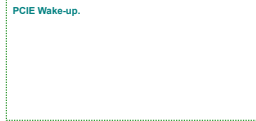
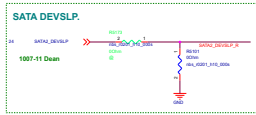
PULL-UP RESISTOR		TEMPERATURE (°C)
ALERT	2KΩ	75
	7.5KΩ	90
	10.5KΩ	100
	14KΩ	105
	18.7KΩ	110

Route CPU_THRM_DA , CPU_THRM_DC and on the same layer

-----OTHER SIGNALS
10 mils
=====GND
10 mils
=====H_THERMDA(10 mils)
10 mils
=====H_THERMDC(10 mils)
10 mils
=====GND
10 mils
-----OTHER SIGNALS
Avoid FSB,Power

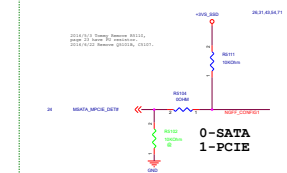
<Variant Name>

SSD CONN.
PCIE colay SATA signals

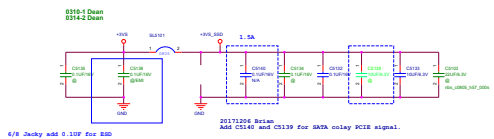


20170628 Brian
Remove PCIE Wake-up schematic select for SSD SATA only.

For PCIE/SATA select.



```
20171206 Brian
Add PCIE/SATA schematic select for SSD SATA colay PCIE.
```



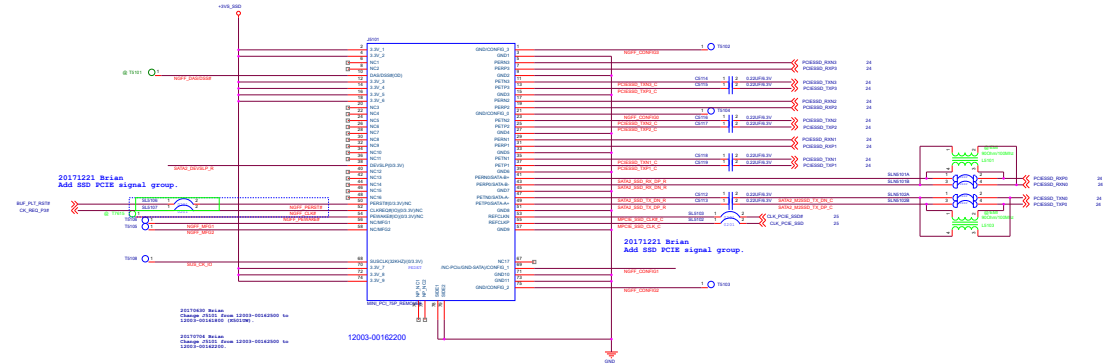
36.3.2.4 AC Capacitor General Guidelines for M.2 SSD Storage Routing on SATA

The following table summarizes the AC capacitor requirements on the motherboard when using the GAT300 half multibay system.

Notes: When SATA and PCIE* are mixed, always route according to SATX design guidelines. SATA does not support signal priority reversal and does not support lane reversal.

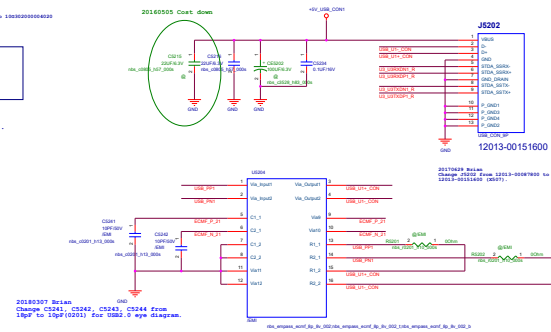
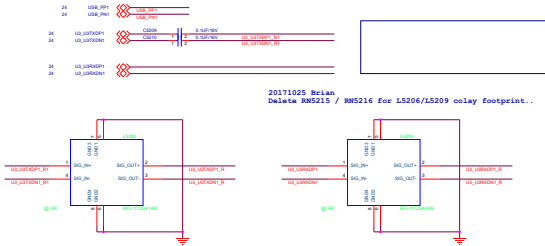
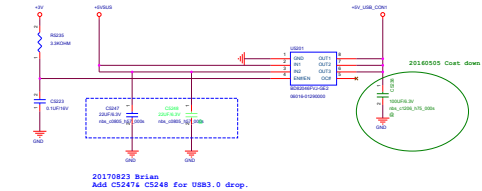
Table 26-2. SATA / PCI Express® Gen 2 and Gen 3 Capacitor Values

Condition	PUL Express [®] line 2 Only	PUL Express [®] line 3 Only	SATX Only	PUL Express [®] line 1/ SATX	PUL Express [®] line 1/ SATX
Pressure To	100 in ²	115 in ²	44 in ²	800 in ²	128 in ²
Pressure At	None	None	10 in ²	None	None ²

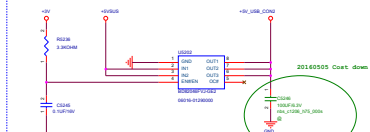


USB3.0_Port 0

USB3.0 port 0 Power SW for Power Protect



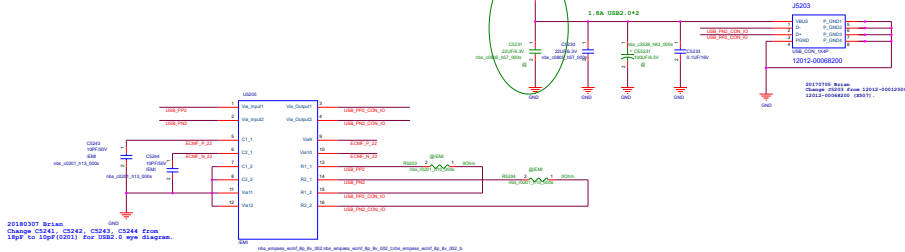
USB2.0 port 2 Power SW for Power Protect



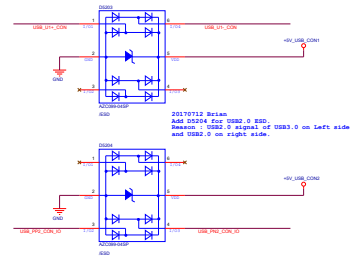
USB2.0_Port 2

X5400J DEL

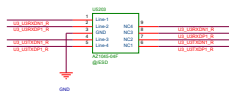
20170505 X5400P2 Add USB2.0

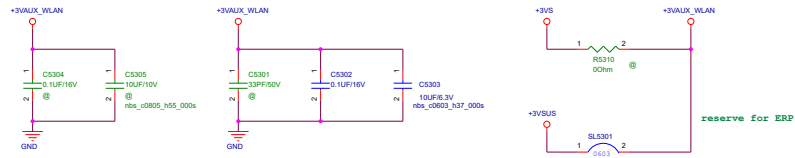


USB 2.0 ESD-Protection

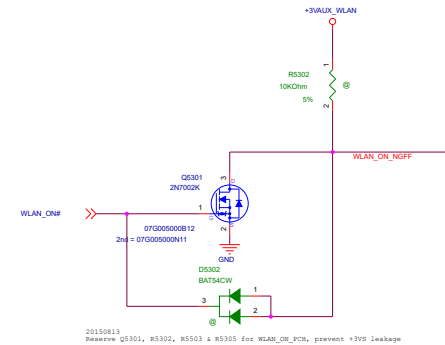
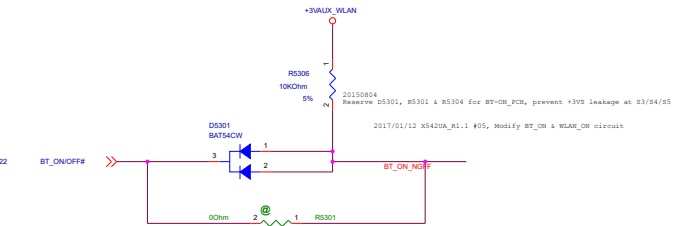


USB3.0 ESD-Protection

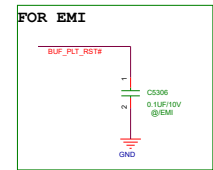
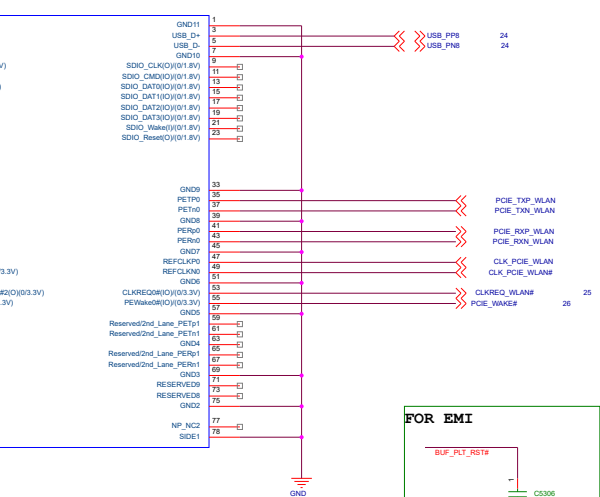
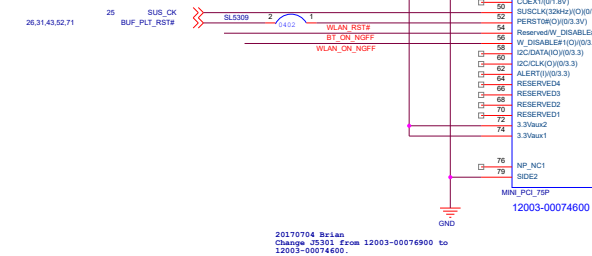




0309-11 Dean cost check keypart list上的WLAN均需+1.5V的需求
=> unstuff C5304, C5305



2017/05/11 Modify R5309 to Shortland SL5309



2017/05/11 BT/WLAN ON OFF Follow X452UQ PR

<Variant Name>

Universal Jack (Normal open type)

R1.3, Item 12.
Add 4 pole headset jack normal open type for project demand.

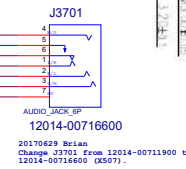
R1.4, Item 13.
Recommend the HP damping resistance 56 ohm for CB certification.
Depend on your project, you can change the resistance value to meet CB certification (under 150mV), best choice is between 140mV-150mV section.

2015/09/24
R2.0 R3709, R3709 change from 51 to 62
Ohm for 音壓測試

20151209 X5411UV 更換PORT

R0.93, Item 3.
Realtek suggest PCB trace width of RING2 & SLEEVE at least 40 mils.

Global Headset
Normal Open
Supported iPhone/Nokia headset, headphone



CITA: 國際標準

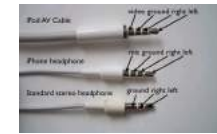
Apple iPhone/HTC/小米的 Phone Jack 定義:

Apple	iPad (Stereo)	iPod (Stereo)	iPhone (Mic)	iPod (AV)
1. Tip	Left channel	Left channel	Left channel	Left channel
2. Ring1	Right channel	Right channel	Right channel	Right channel
3. Ring2	-	-	Ground	Ground
4. Sleeve	Ground	Ground	Mic	Video

OMTP: 國家標準

Nokia Type 的 Phone Jack 定義:

Standard	Mono	Stereo	Stereo + Mic	Audio + Video
1. Tip	Left channel	Left channel	Left channel	Left channel
2. Ring1	-	Right channel	Right channel	Video
3. Ring2	-	-	Mic	Ground
4. Sleeve	Ground	Ground	Ground	Right channel



耳機pop noise mute線路

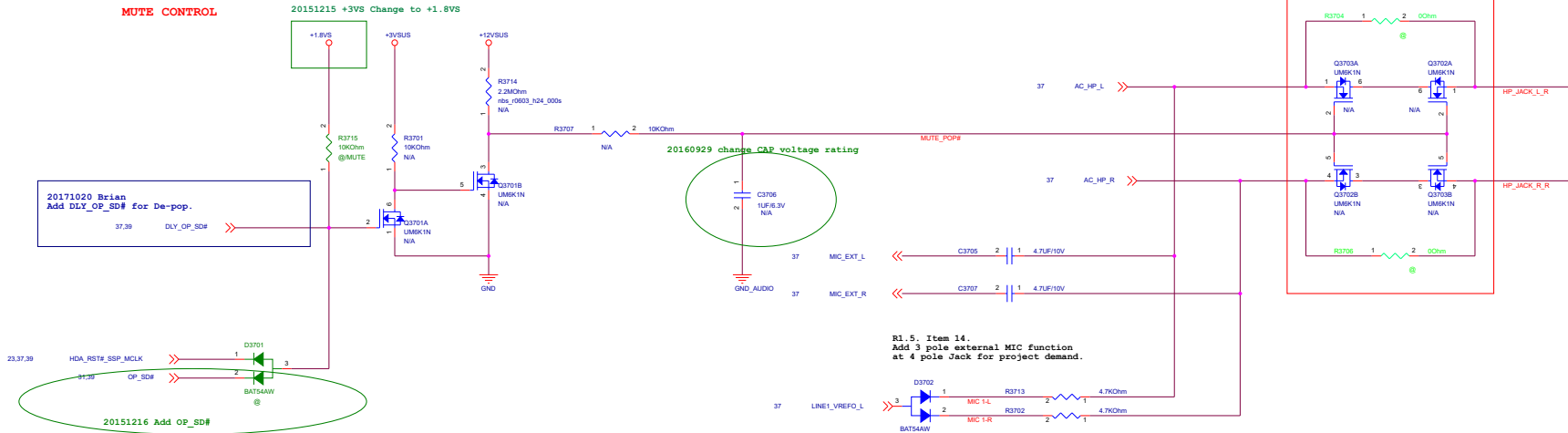
MUTE CONTROL

20151215 +3VS Change to +1.8VS

20160929 change CAP voltage rating


R1.5, Item 14.
Add 3 pole external MIC function at 4 pole Jack for project demand.

MUTE CONTROL



BOM

Project Name		Rev
ASUS X407UA/UV		R1.0
Title : IO Board-Audio Jack		
Dept:	ASUSTek COMPUTER INC. Engineer:	Brian Chen
Date: Wednesday, March 07, 2018	Sheet	38 of 102

 Project Name X407UA/UV		Rev R1.0
Title : ASM1142_USB3.1_TYPEC		
Size C	Dept.: ASUSTeK COMPUTER INC. Engineer: Brian Chen	
Date: Wednesday, March 07, 2018	Sheet	55 of 102



Project Name

X407UA/UV

Rev

R1.0

Title : **USB 3.1 MB Type-C**


Size

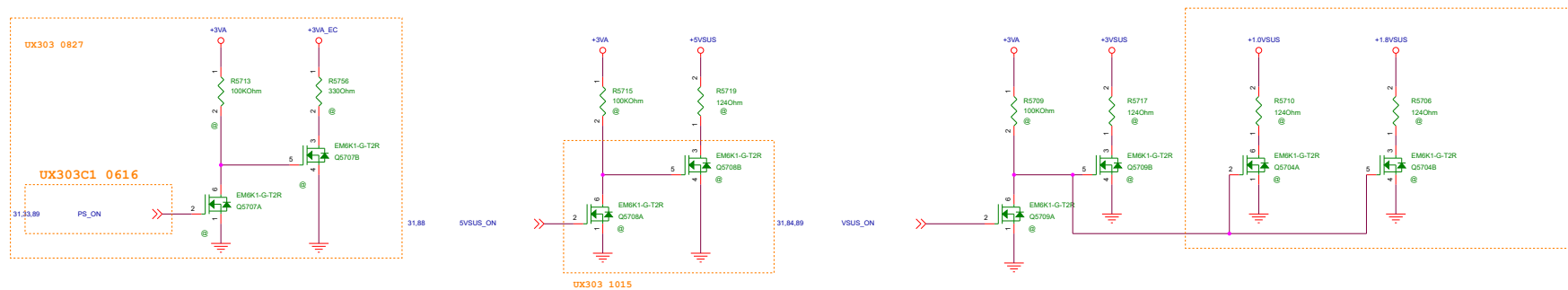
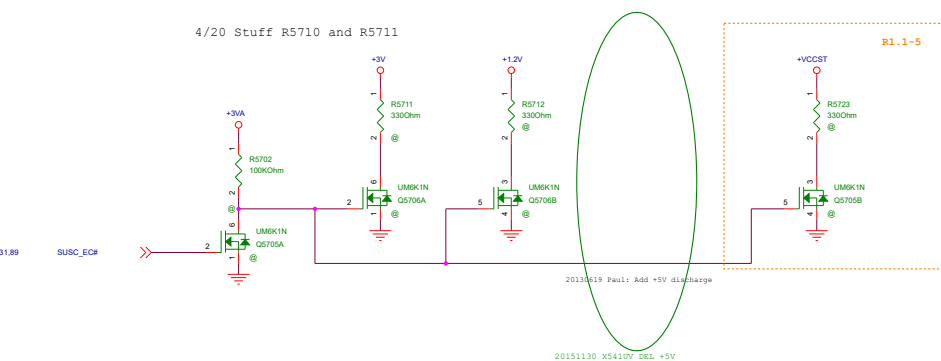
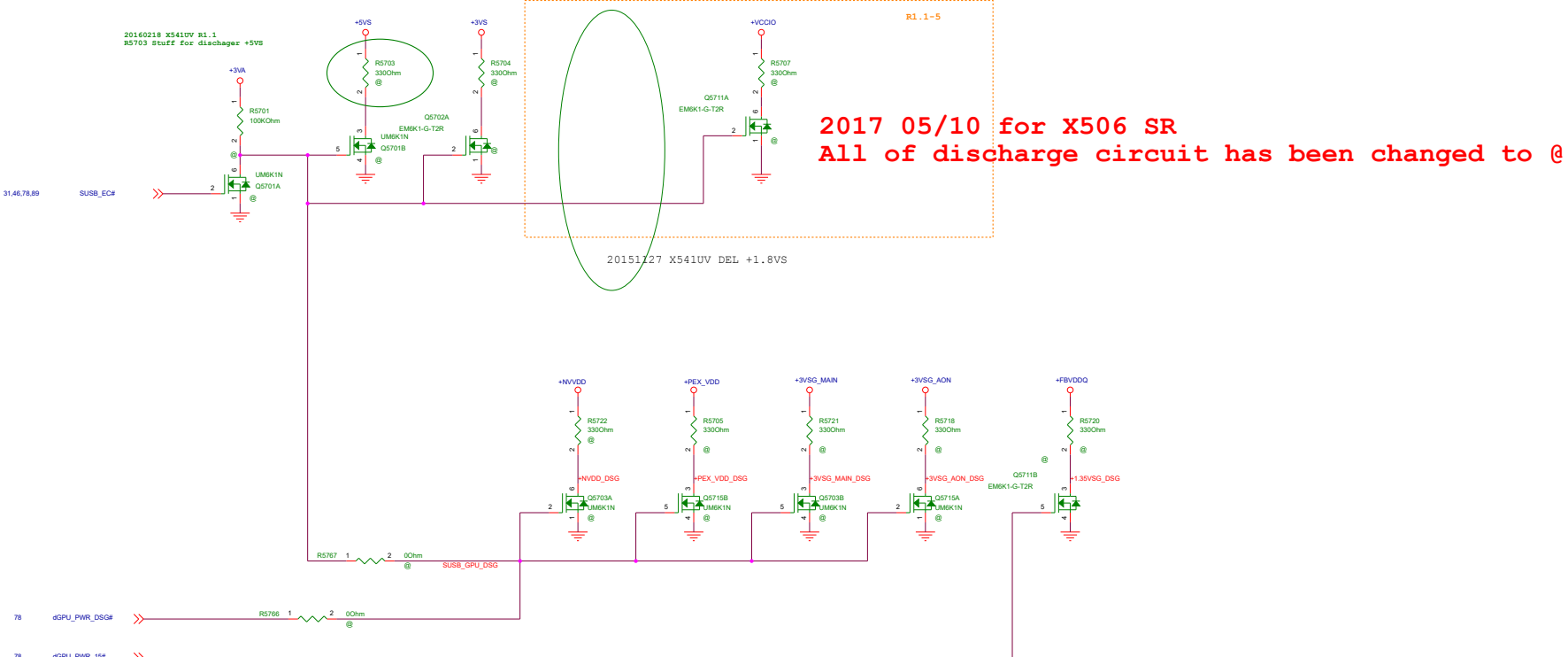
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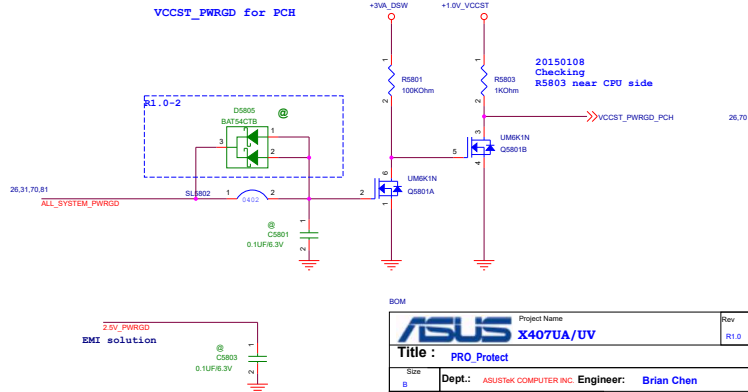
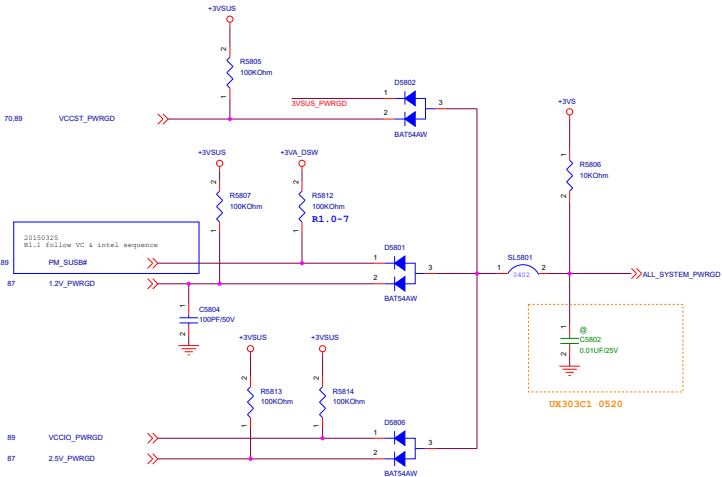
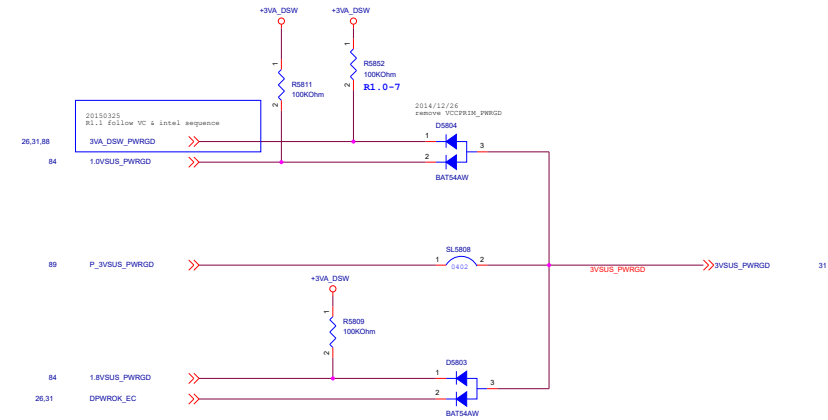
Dept.: **ASUSTeK COMPUTER INC. NB1** **Engineer:** **Brian Chen**

Date: **Wednesday, March 07, 2018**

Sheet **56** of **102**

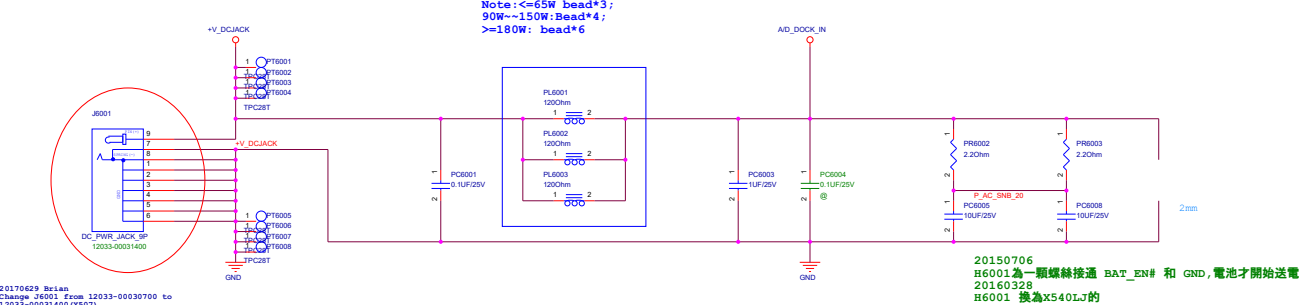
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Title : PWR_SW&HALL_SW				
Size A	Dept.: ASUSTeK COMPUTER INC. Engineer: Brian Chen			
Date: Wednesday, March 07, 2018			Sheet	57 of 102





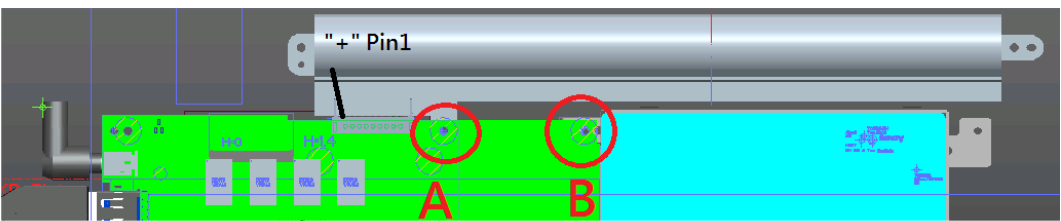
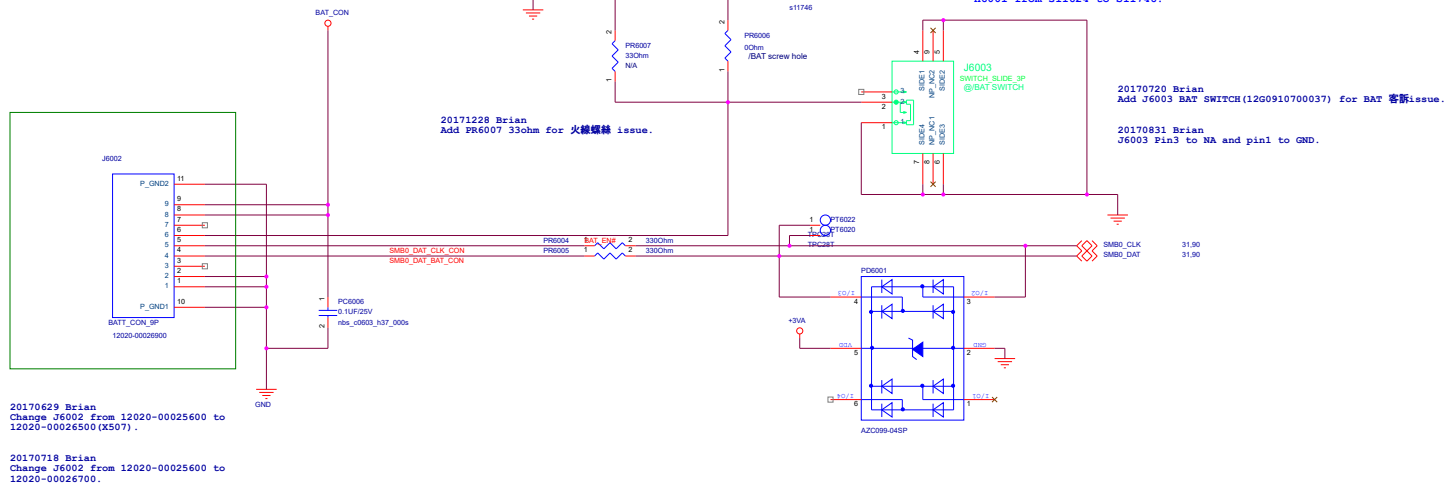
BOM

ASUS		Project Name	Rev
X407UA/UV			R1.0
Title : PRO_Protect			
Size	Dept.:	ASUSTek COMPUTER INC.	Engineer: Brian Chen
Date: Wednesday, March 07, 2018	Sheet	59	of 102





換Connector 整個 GND Shape 都要跟PIN腳連起來


Battery Connector





Pin Seq.	Name	Description	Remark
1	P+	Battery pack positive terminal	Output voltage
2	P+	Battery pack positive terminal	Output voltage
3	NC		
4	EN#	External charge & discharge Mosfet control pin.	SYSTEM Connection to GND for charge & discharge (Enable Function)
5	SMBC	Serial clock input	SMBC
6	SMBD	Serial data input	SMBD
7	NC		
8	P-	Battery pack negative terminal	GND
9	P-	Battery pack negative terminal	GND


		Project Name		Rev
		X407UA/UV		R1.0
Title : Sensors				
Size Custom	Dept.: ASUSTeK COMPUTER INC. Engineer: Brian Chen			
Date: Wednesday, March 07, 2018			Sheet	62 of 102

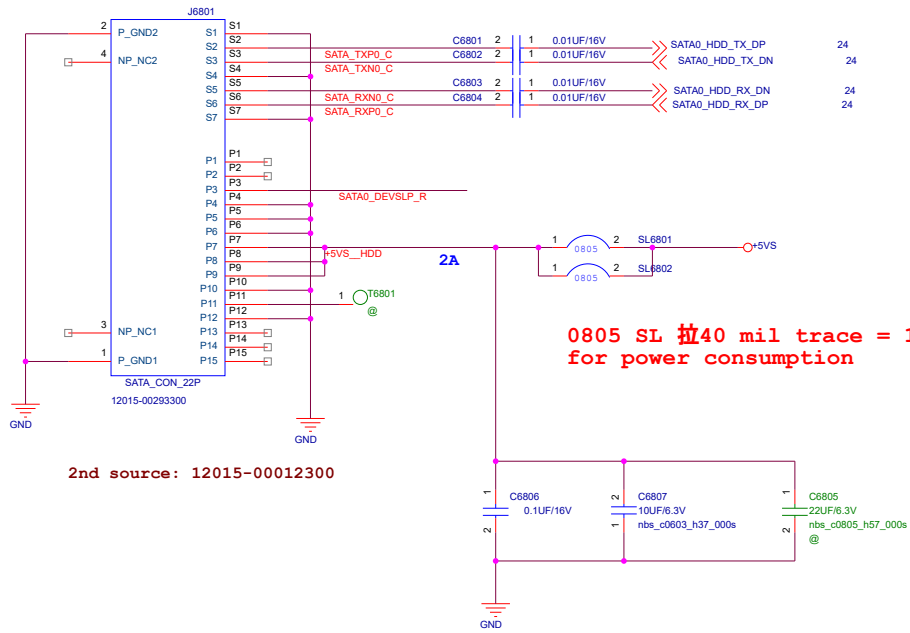
		Project Name		Rev
		X407UA/UV		R1.0
Title : ****				
Size C	Dept.: ASUSTeK COMPUTER INC. Engineer: Brian Chen			
Date: Wednesday, March 07, 2018			Sheet	63 of 102

		Project Name		Rev
		X407UA/UV		R1.0
Title : NFC				
Size Custom	Dept.: ASUSTeK COMPUTER INC. Engineer: Brian Chen			
Date: Wednesday, March 07, 2018			Sheet	64 of 102

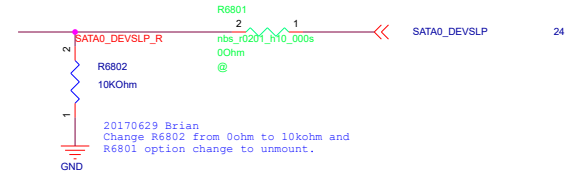
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		X407UA/UV		R1.0
Title : IO_SATA HDD & SPEAKER				
Size Custom	Dept.: ASUSTeK COMPUTER INC. Engineer: Brian Chen			
Date: Wednesday, March 07, 2018			Sheet	65 of 102

		Project Name		Rev
		X407UA/UV		R1.0
Title : IO_USB				
Size				
C	Dept.:	ASUSTeK COMPUTER INC.	Engineer:	Brian Chen
Date: Wednesday, March 07, 2018			Sheet	67 of 102

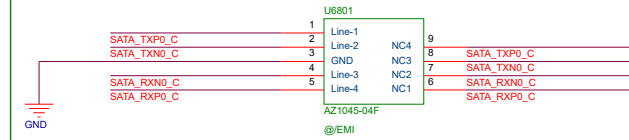
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		X407UA/UV		R1.0
Title : IO_USB*2 & CR & LED				
Size C	Dept.: ASUSTeK COMPUTER INC. Engineer: Brian Chen			
Date: Wednesday, March 07, 2018			Sheet	68 of 102



SATA DEVS LP.



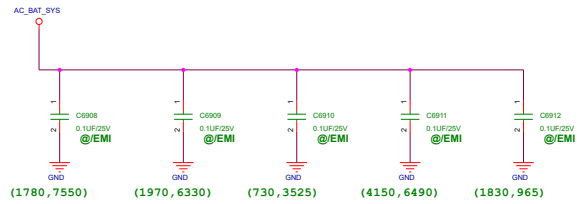
FOR EMI



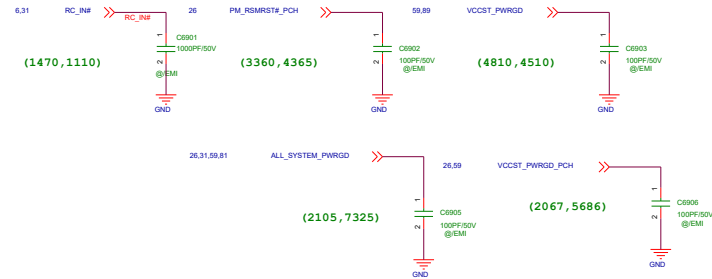
BOM

Project Name		Rev
ASUS X407UA/UV		R1.0
Title : B TO B CONNECTOR		
Size	Dept.:	Engineer: Brian Chen
B	ASUSTek COMPUTER INC.	
Date: Wednesday, March 07, 2018	Sheet	69 of 102

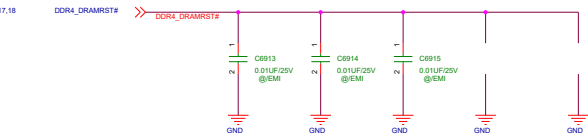
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EMI CAP



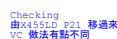
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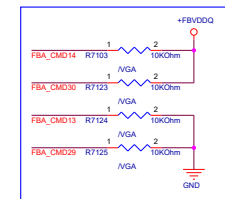


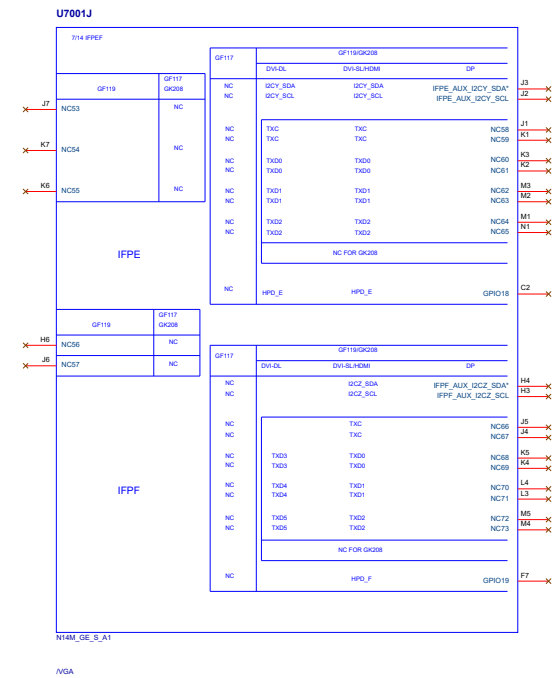
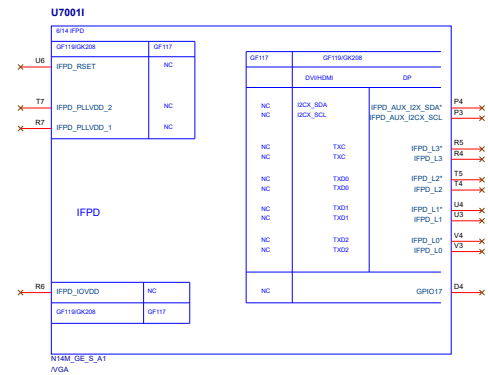
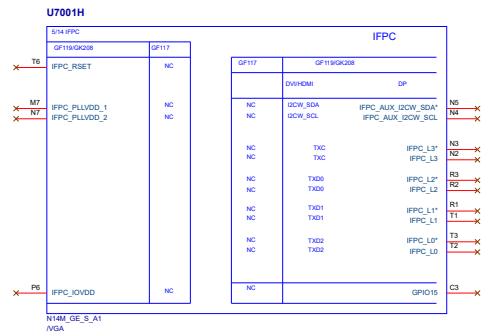
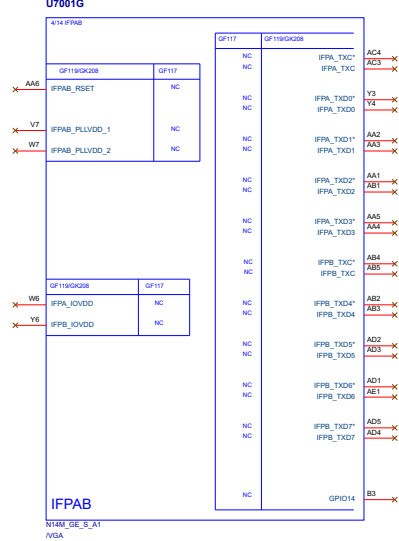
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BOM

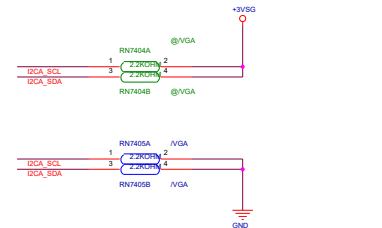
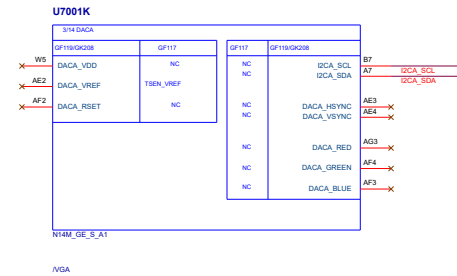
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X407UA/UV			R1.0
Title : EMI			
Size	Dept.	ASUS/tek COMPUTER INC.	Engineer: Brian Chen
C			
Date: Wednesday, March 07, 2018	Sheet	70	of 102







CRT

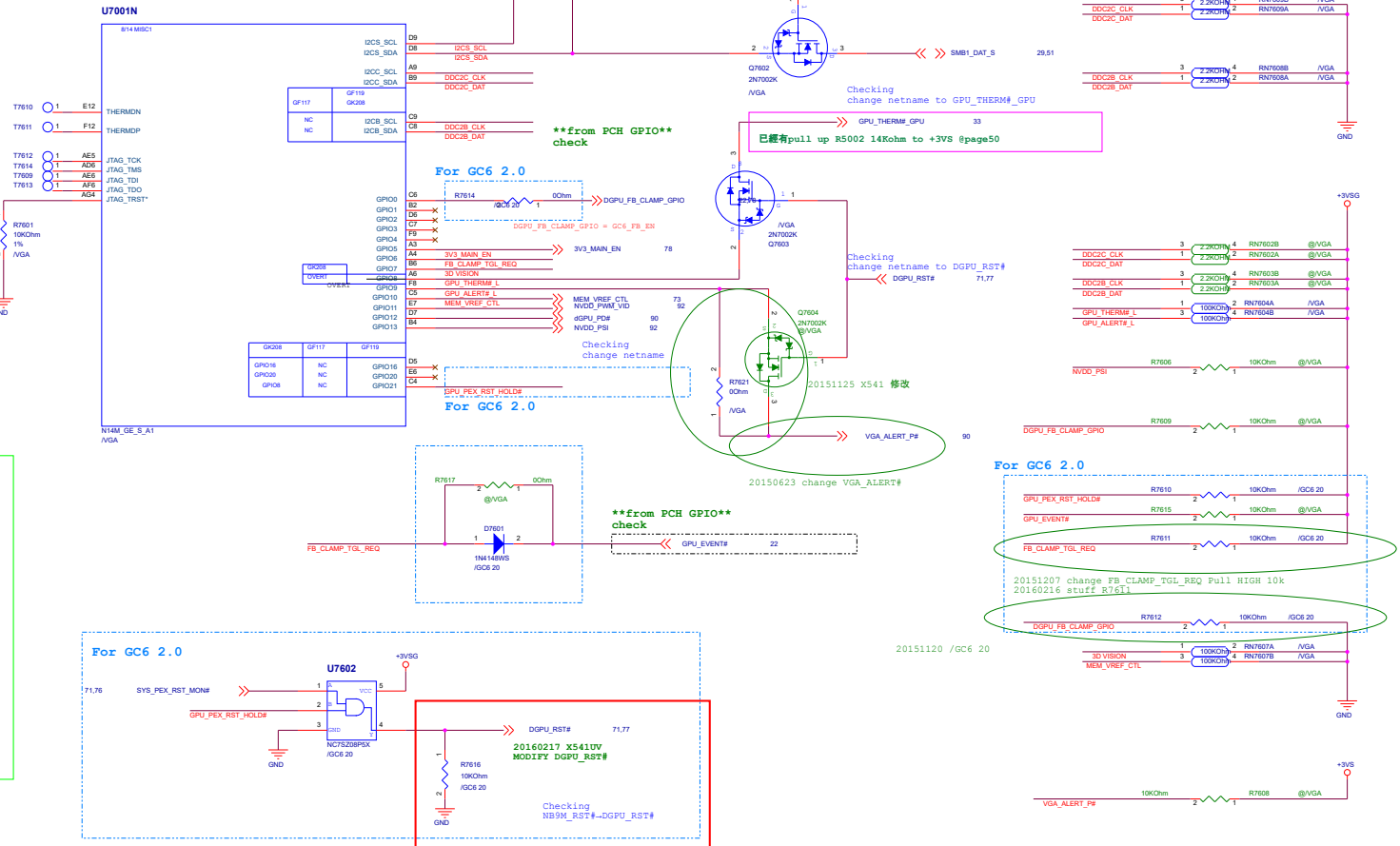



BCM


Table 12-1. GB2B-64 and GB4B-128 GPIO Description

Pin Name	Normal Function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	FB_CLAMP_AONH	I	FB Clamp monitor for GC6 1.0	
	GC6_FB_EN	O	FB Enable for GC6 2.0	100K pull-down to GND
GPIO1	MEM_VDD_CTL	O	Memory VDD VDD	MEM VDD: pull-up to 3V3_AOH or pull-down to GND to set boot FBVDD/Q voltage
GPIO2	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control	100K pull-down
GPIO3	LCD_VCC	O	Panel Power Enable	LCD_VCC: 100K pull-down
GPIO4	LCD_BLED	O	Panel Backlight Enable	100K pull-down
GPIO5	3V3_MAIN_EN	O	GPU power sequencing	100K pull-up to 3V3_AOH
GPIO6	FB_CLAMP_TGL_REQ	O	Clamp/toggle request for GC6 1.0	100K pull-up to system 3.3V
	GPU_EVENT#	I	GPU wake signal for GC6 2.0	100K pull-up to 3V3_AOH
GPIO7	3D Vision	O	3D Vision L/R signal	100K pull-down
GPIO8	SYS_PEX_RST_MON#	I	System side PCIe reset Monitor	
GPIO9	ALERT	I/O	Active Low Thermal Alert	100K pull-up to 3V3_AOH
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100K pull-down
GPIO11	PWM_VDD	O	GPU Core VDD PWM control signal	
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100K pull-up to 3V3_AOH
GPIO13	PSI	O	Phase Shedding	100K pull-up to 3V3_AOH to enable two phase.
GPIO14	HPD_A	I	Hot Plug Detect for IFPA used as DisplayPort or for BPFA8 when used as Dual Link DVI	See Figure 12-1
GPIO15	HPD_C	I	Hot Plug Detect for IFPC	See Figure 12-1
GPIO16	RESERVED			
GPIO17	HPD_D	I	Hot Plug Detect for IFPD	See Figure 12-1
GPIO18	HPD_E	I	Hot Plug Detect for IFPE	See Figure 12-1
GPIO19	HPD_F or HPD_B	I	Hot Plug Detect for IFPF or for IFPB when used as DisplayPort	See Figure 12-1
GPIO20	Reserved			
GPIO21	GPU_PEX_RST_HOLD#	O	GPU PCIe soft-reset control	100K pull-up to 3V3_AOH
OVERT	OVERT	O	Active Low Thermal Catastrophic Over Temperature	100K pull-up to 3V3_AOH

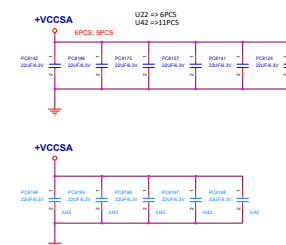
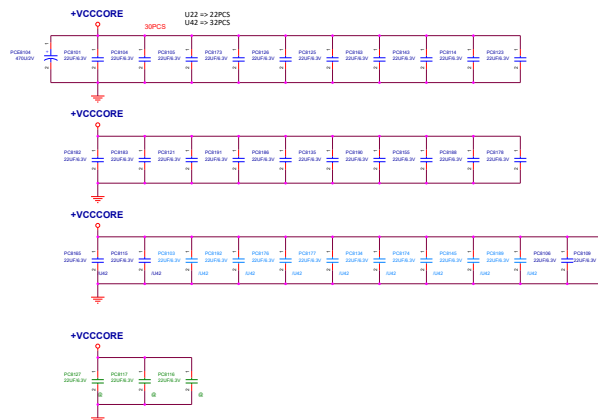
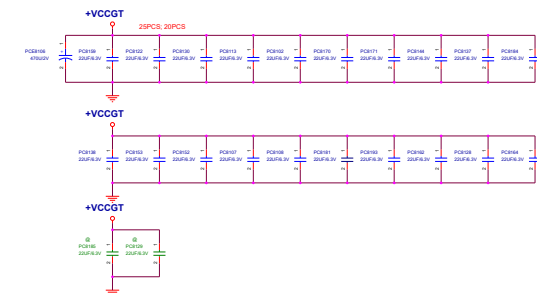
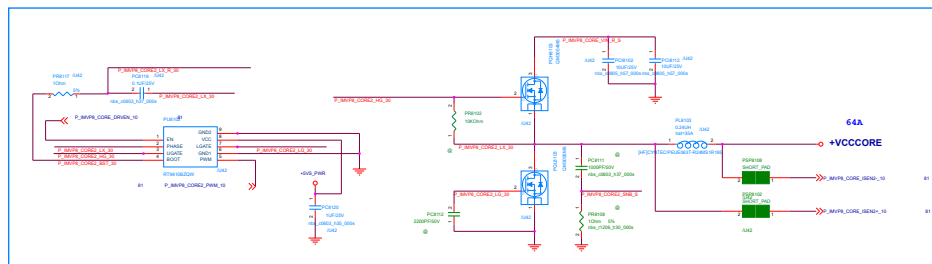
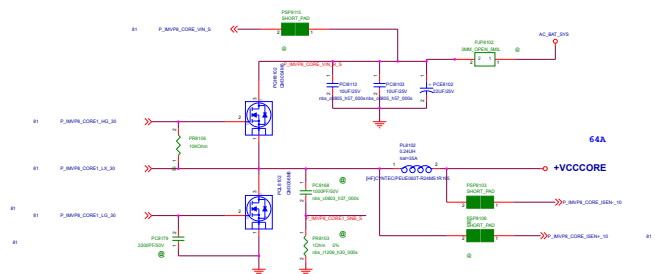
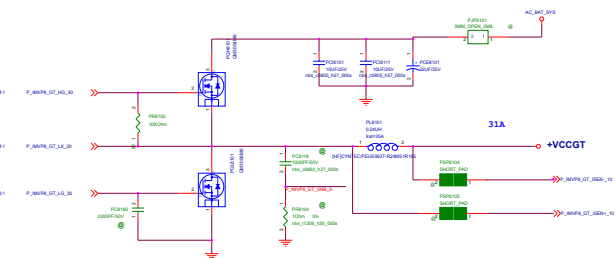
GPIO





		Project Name		Rev
		X407UA/UV		R2.0
Title : VGA_****				
Size				
C	Dept.: ASUSTeK COMPUTER INC.		Engineer: Brian Chen	
Date: Wednesday, March 07, 2018			Sheet	79 of 102

		Project Name		Rev
		X407UA/UV		R1.0
Title : VGA_****				
Size C	Dept.: ASUSTeK COMPUTER INC. Engineer: Brian Chen			
Date: Wednesday, March 07, 2018			Sheet	80 of 102

Kaby Lake-U IMVP8 Power (2) [For CPU]



		Project Name		Rev
		X540UVK		R1.0
Title : PW_SKYLAKE-U (3)				
Size Custom	Dept.: NB Power Team		Engineer:	Andy
Date: Wednesday, March 07, 2018			Sheet	83 of 102

		Project Name		Rev
		X540UVK		0.9
Title : POWER_+VGFX_CORE				
Size Custom	Dept.: ASUSTeK COMPUTER INC. Engineer: Andy			
Date: Wednesday, March 07, 2018			Sheet	93 of 102

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		Project Name		Rev
		X407UA/UV		0.9
Title : POWER_+VGFX_CORE				
Size Custom	Dept.: ASUSTeK COMPUTER INC. Engineer: Power			
Date: Wednesday, March 07, 2018			Sheet	95 of 102

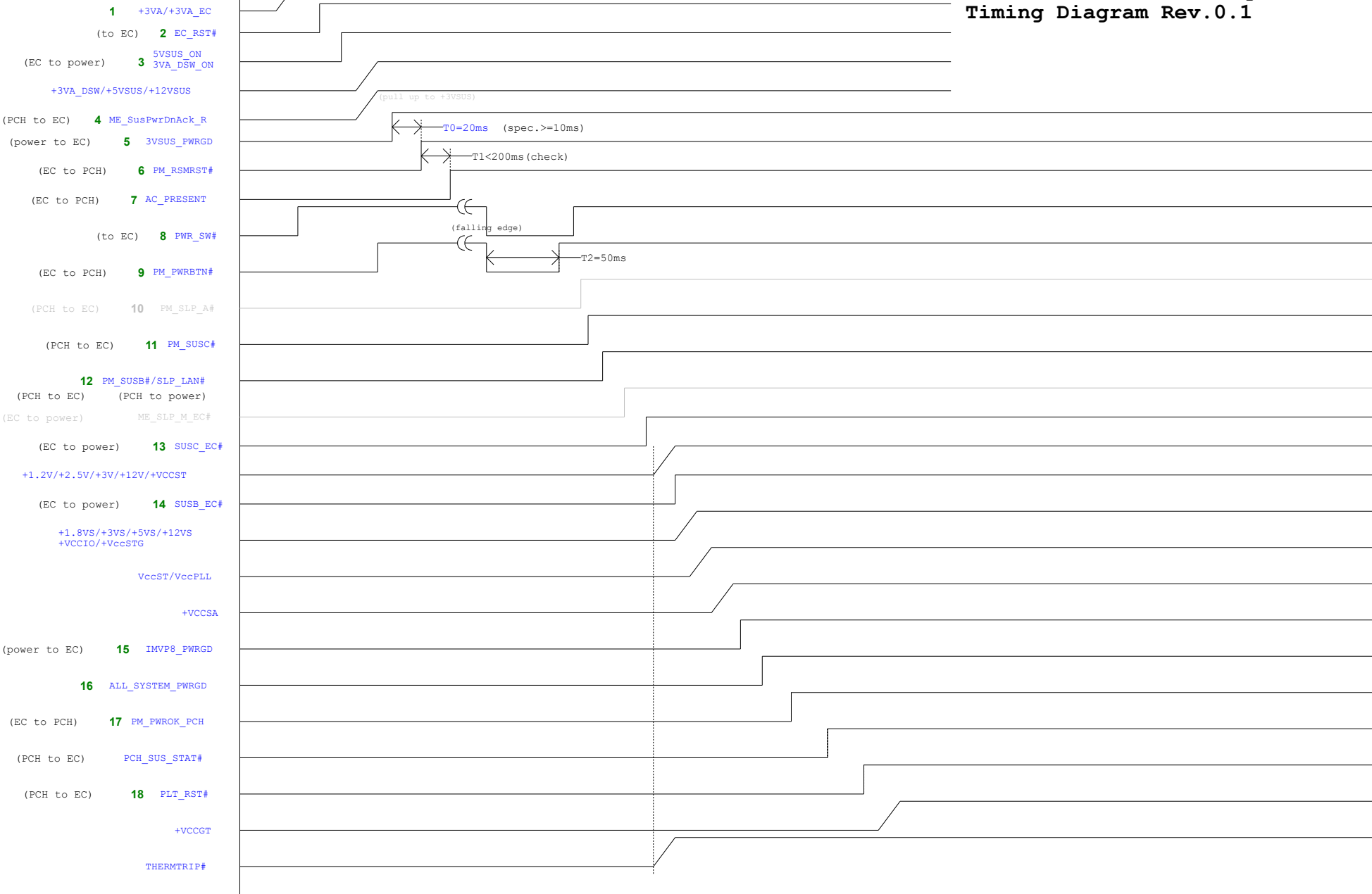
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Title : POWER_+VGFX_CORE				
Size Custom	Dept.: ASUSTeK COMPUTER INC. Engineer: Power			
Date: Wednesday, March 07, 2018			Sheet	96 of 102

		Project Name		Rev
		X407UA/UV		0.9
Title : POWER_+VGFX_CORE				
Size Custom	Dept.: ASUSTeK COMPUTER INC. Engineer: Power			
Date: Wednesday, March 07, 2018			Sheet	97 of 102

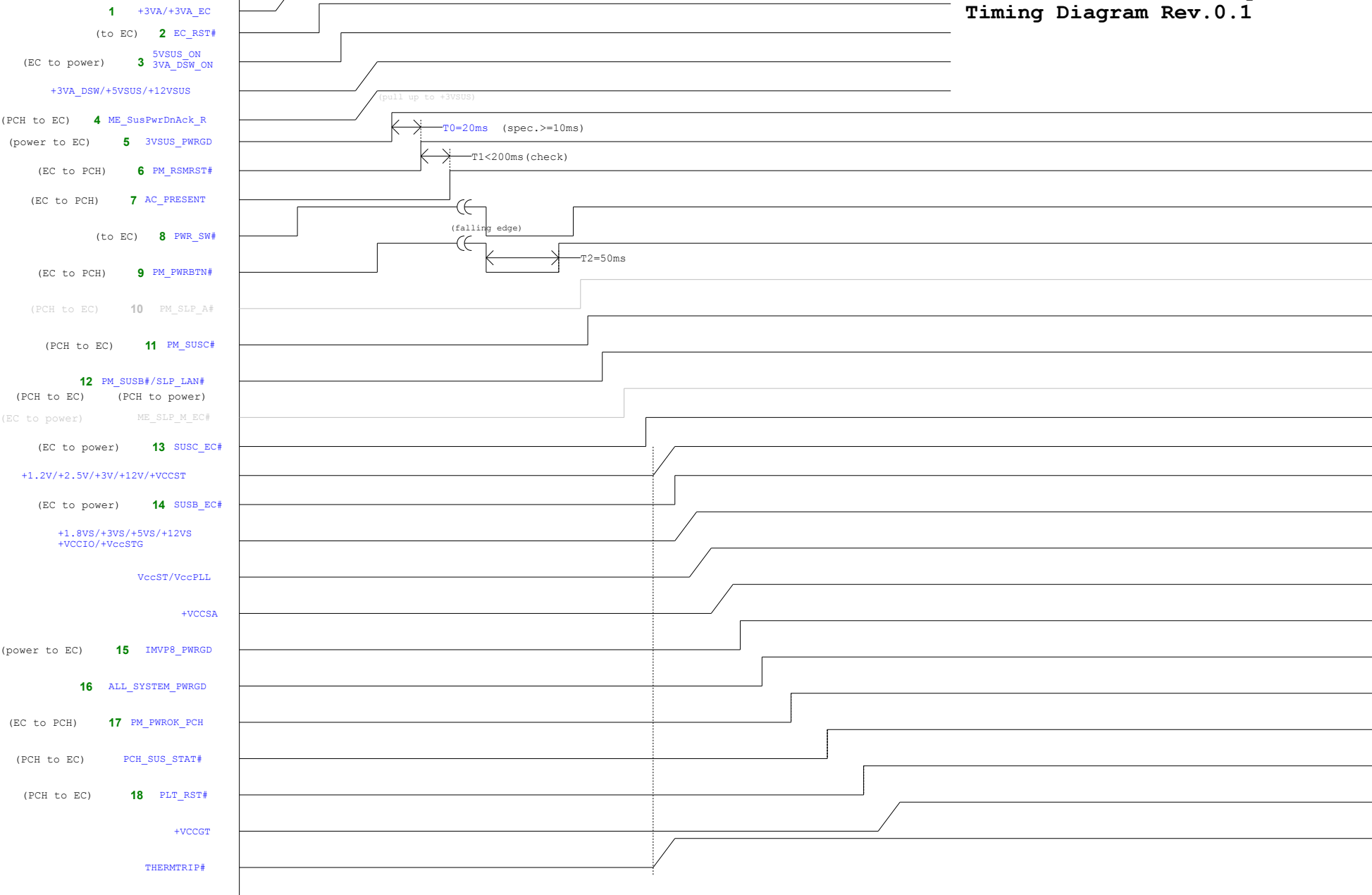
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Title : POWER_+VGFX_CORE				
Size Custom	Dept.: ASUSTeK COMPUTER INC. Engineer: Power			
Date: Wednesday, March 07, 2018			Sheet	98 of 102

		Project Name		Rev
		X407UA/UV		0.9
Title : POWER_+VGFX_CORE				
Size Custom	Dept.: ASUSTeK COMPUTER INC. Engineer: Power			
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BOM



BOM

Load Switch

